Realization of reliable and flexible logic gates using noisy nonlinear circuits

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It was shown recently [Murali *et al.*, Phys. Rev. Lett. **102**, 104101 (2009)] that when one presents two square waves as input to a two-state system, the response of the system can produce a logical output (NOR/OR) with a probability controlled by the interplay between the system noise and the nonlinearity (that characterizes the bistable dynamics). One can switch or "morph" the output into another logic operation (NAND/AND) whose probability displays analogous behavior; the switching is accomplished via a controlled symmetry-breaking dc input. Thus, the interplay of nonlinearity and noise yields flexible and reliable logic behavior, and the natural outcome is, effectively, a logic gate. This "logical stochastic resonance" is demonstrated here via a circuit implementation using a linear resistor, a linear capacitor and four CMOS-transistors with a battery to produce a cubiclike nonlinearity. This circuit is simple, robust, and capable of operating in very high frequency regimes; further, its ease of implementation with integrated circuits and nanoelectronic devices should prove very useful in the context of reliable logic gate implementation in the presence of circuit noise. © *2009 American Institute of Physics*. [doi:10.1063/1.3245318]

In recent years it has become increasingly evident that the interplay of noise and nonlinearity in a dynamical system can produce interesting counterintuitive phenomena. Stochastic resonance (SR) provides one such example, wherein noise and nonlinear dynamics cooperate to yield an enhancement of the system response for an optimal value of the noise intensity.[1] Recently, we investigated a variation of the SR effect in a simple threshold detector subject to the superposition of two random square waves. We found that, *in an optimal band of noise*, the output was a logical combination of the two input signals, an effect that we have termed logical SR (LSR). Our interest in this problem stems from an issue that is receiving considerable attention today: as computational devices and platforms continue to shrink in size and increase in speed we are increasingly encountering fundamental noise characteristics that cannot be suppressed or eliminated.

The most direct way to realization of LSR is via analog circuits, such as the one described in Ref. 2. However, such circuits are not useful for applications, due to the complex construction of every unit, which results in very bulky and complicated circuits. Hence it is of considerable importance to look for simpler (and, hence, smaller) electronic circuit models; this also has the effect of lowering the circuit noise floor. Here, we present an electronic circuit with CMOS transistors for the observation and implementation of LSR.

Logical stochastic resonance: Considers a general nonlinear dynamic system given by $\dot{x}=F(x)+I+D\eta(t)$, where $F(x)$ is a generic nonlinear function obtained as the gradient of a bistable potential energy function, I is a low amplitude dc input signal, $\eta(t)$ is an additive zero-mean Gaussian noise with unit variance and intensity D; the noise is taken to have correlation time smaller than any other time scale in the system, so that it may be represented, theoretically, as delta correlated.

Usually, a logical input-to-output correspondence is achieved by encoding N inputs in N square waves. Specifically, for two logic inputs encoded in the aperiodic pulses $I_{1,2}$, we drive the system with the summed (low amplitude) signal I. The logic inputs can be either 0 or 1, giving rise to 4 distinct logic input sets $(I_1,I_2):(0,0),(0,1),(1,0),(1,1)$. One readily observes that the four distinct input conditions for (I_1,I_2) yield an input signal I that is a three-level aperiodic waveform.

The output of the system is determined by its state e.g., the output can be considered a logical 1 if it is in one well, and logical 0 in the other well. Specifically, the output corresponding to this two-input set, for a system with potential wells at $x_+>0$ and $x_-<0$, is taken to be 1 (or 0) when the system is in the well at x_+, and 0 (or 1) when the system is in the other well. Hence, when the system switches wells, the output is "flipped." We have, already, demonstrated[2] that one observes, for a given set of inputs (I_1,I_2), a *logical* output

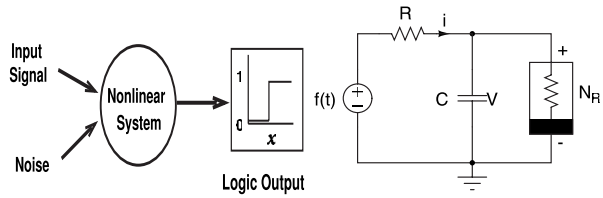

FIG. 1. Schematic diagram of (left) logic cell comprised of a nonlinear system forced by an input signal $(I=I_1+I_2+\varepsilon)$ and noise (right) circuit diagram for LSR system. Here $f(t)=I_1+I_2+\varepsilon+$ noise, N_R is the nonlinear element, R and C are linear resistor and capacitor, respectively.

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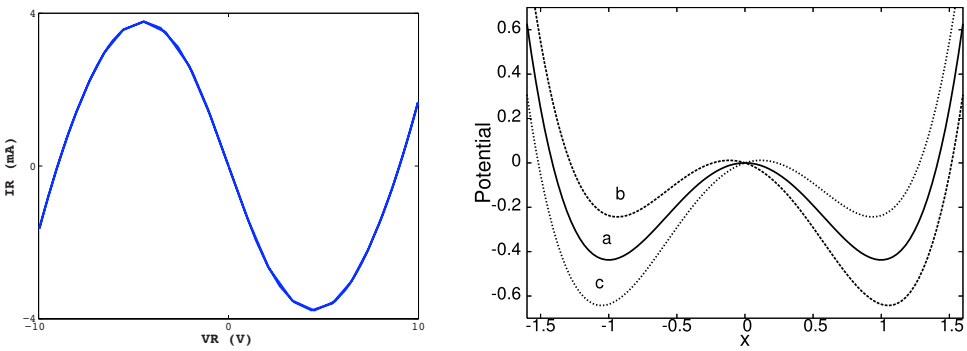

FIG. 2. (Color online) (left) Simulated cubiclike driving point characteristic curve of nonlinear resistor N_R (right) effective potential well arising in Eq. (2), with additional constant bias (a) $\varepsilon=0$ (symmetric well), (b) $\varepsilon=+0.2$, and (c) $\varepsilon=-0.2$.

from this nonlinear system, in accordance with the truth tables[3] of the basic logic operations. Most importantly, this occurs consistently and robustly only in an optimal window of noise. For very small or very large noise the system does not yield any consistent logic output, in line with the basic tenets of SR. But in a reasonably wide band of moderate noise, the system produces the desired logical outputs consistently.

CMOS based circuit: In this letter, we propose a simple CMOS based circuit, with few circuit elements, to observe and exploit LSR (shown schematically in Fig. 1). Our circuit consists of a linear resistor R, linear capacitor C, and a nonlinear (constructed to be cubic) circuit element [Fig. 2(a)] implemented using CMOS transistors. The circuit can be visualized as a pair of cross-coupled CMOS inverters (CD4007CN), as shown in Fig. 3. This subcircuit is characterized by low parasitic capacitance and, when used as a cubic-nonlinear element, the resulting circuit can operate across a *very high frequency range*.[4] We construct this element with a dual complementary pair plus inverter chip[4] powered by single 9 V battery. To achieve maximum speed of operation using this nonlinearity, the parasitic capacitance across its terminals was used as the circuit element ($C=49$ pF) in the LSR circuit of Fig. 1 (right). The governing circuit equations are

$$RC\frac{dV}{dt} = -V - Rg(V) + f(t), \tag{1}$$

where $f(t)=D\eta(t)+I_1+I_2+\varepsilon$ and $g(V)$ is the driving-point characteristic of the nonlinear resistor represented as a smooth cubic nonlinearity $g(V)=G_aV-(G_a/V_{\max}^2)V^3$, with G_a being the (experimentally measured) slope, at the origin, of the nonlinearity. The change to dimensionless variables $x=(V/V_{\max}), \tau=(t/RC), a=(G_a/G), G=(1/R)$ leads to an equation that is convenient for analysis and numerical simulation:

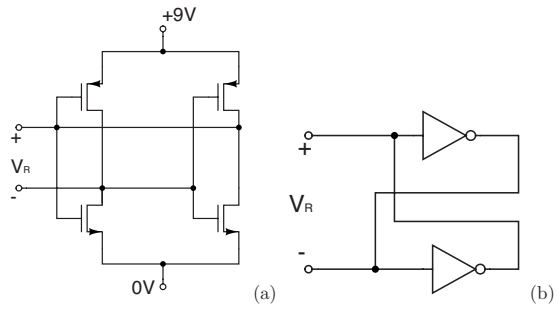

FIG. 3. (a) Four transistor cubiclike nonlinear resistor N_R (b) Cross coupled two inverter implementation of nonlinear resistor N_R.

$$\dot{x} = f(\tau) - \alpha x + \alpha x^3, \tag{2}$$

with the definitions $\alpha=1+a$ and $f(\tau)=I_1+I_2+\varepsilon+D\eta(t)$. We note that Eq. (2) is the prototype overdamped system with dynamics derived from the bistable quartic potential $U(x)=\alpha[-(x^2/2)+(x^4/4)]$, this system exhibits SR for the appropriate choices of system and noise parameters.[1] Absent the forcing function $f(\tau)$, the switching between the stable states $x_\pm=\pm\sqrt{\alpha/2a}$ is noise driven if $D\neq 0$.

Results: We are, now, in position to describe the results of experiments carried out using the circuit of Fig. 2. With no loss of generality, consider two (randomly switched) inputs $I_{1,2}$ to take the value -0.2 V when the logic input is 0, and the value 0.2 V when the input is 1. Then, the input signal $I=\varepsilon+I_1+I_2$ is a three-level aperiodic square wave form. We reiterate that ε is the additional constant input bias (over a temporal interval much longer than the noise correlation time) which introduces asymmetry in potential function $U(x)$. In Fig. 4 we show the response of the system (1) for $\varepsilon=0.2$ V and three choices of noise intensity D. We observe that, under optimal noise, interpreting the capacitor voltage $V<0$ as logic output 0 and the voltage $V>0$ as logic output 1 yields a clean (i.e., stable) logical OR whereas interpreting the capacitor voltage $V>0$ as logic output 0 and $V<0$ as

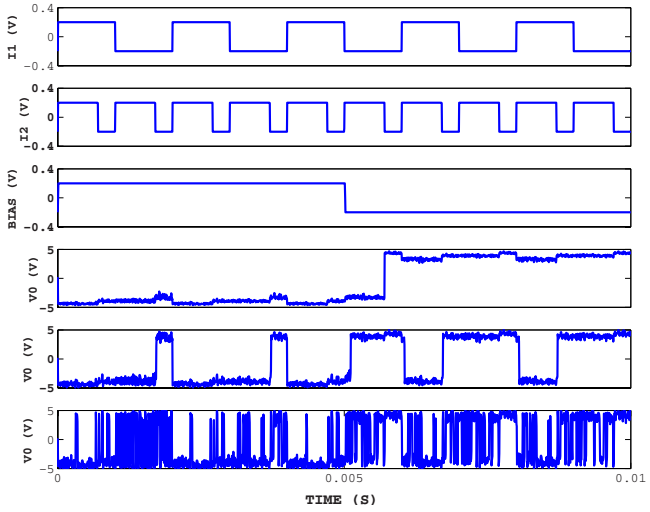

FIG. 4. (Color online) Density map of P (logic) for the (left) NOR and (right) NAND logic operation, as functions of the noise intensity (x-axis) and asymmetrizing dc input (y-axis) obtained from numerical simulations. Reliable NAND performance accrues for $\varepsilon\sim-0.2$; for reliable NOR performance, $\varepsilon\sim+0.2$. Optimal performance in both cases is obtained for D values lying within the optimal window. Note that, for D outside the optimal window, one can still, for any D, optimize NAND/NOR performance by adjusting ε (this amounts to an adjustment of the asymmetry in nonlinearity for a given system noise floor).

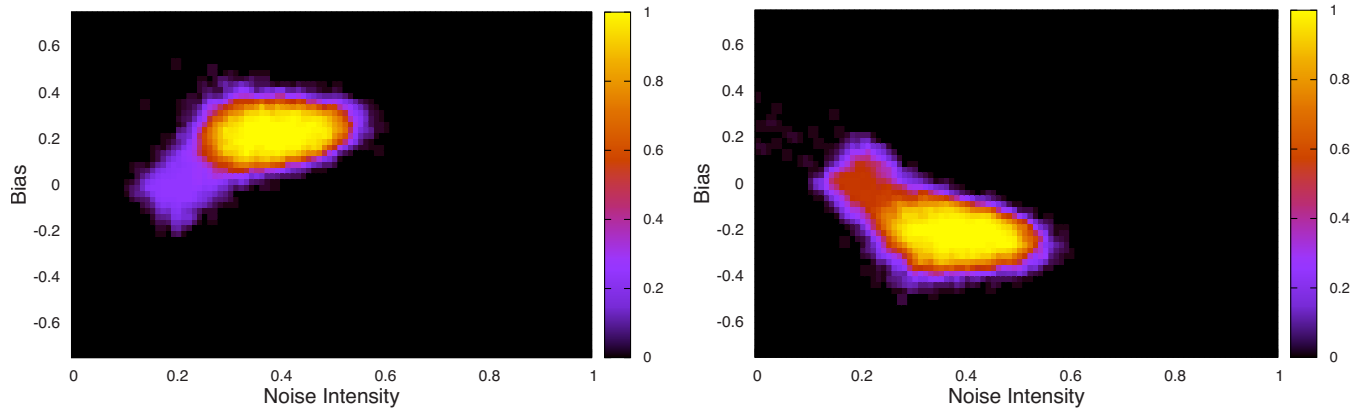

FIG. 5. (Color online) Experimental circuit results. From top to bottom: panels 1 and 2 show streams of inputs I_1 and I_2, which take value 0.2 V when logic input is 0 and value 0.2 V when logic input is 1. Panel 3 shows the constant bias signal varying from 0.2 V (0–5 ms) to −0.2 V (5–10 ms). Panels 4, 5, and 6 show the waveforms of $V_0=-V_c(t)$ obtained from the circuit of Fig. 2 under noise levels D: (i) 0.4 V, (ii) 1 V, and (iii) 2 V. When the noise levels is in an optimal band, $D=1$ V, the desired NOR logic output (when $\varepsilon=0.2$ V) or NAND logic output (when $\varepsilon=0.2$ V), while for small or larger noise, one does not obtain the necessary response.

logic output 1 yields a clean logical NOR. In a completely analogous way, by setting the asymmetry value $\varepsilon=-0.2$ V, we can realize clean AND and NAND gates in almost the same optimal noise intensity regime as the previous case. Note that NAND and NOR are fundamental logic gates which can, in combination, yield all possible logical responses.

The observations above, can be explained in the standard framework of SR.[1] The different outputs, obtained by driving the state of the system to one or the other well, are realized by appropriately manipulating the asymmetry of the wells. One can, then, readily understand the occurrence of a particular logic output: when the inputs $I_{1,2}$ are added, the effective positions of the potential minima (as well as the energy barrier height separating them) change. This asymmetry causes the state variable to switch to the desired well under adequate noise. For $\varepsilon>0$ one obtains the NOR logic operation, and for $\varepsilon<0$ one obtains the NAND logic operation.

We can quantify the consistency (or reliability) of obtaining a given logic output by calculating the probability of obtaining the desired logic output for different input sets to Eq. (2) through numerical simulation with the rescaled parameters $\alpha=-1.75, a=-2.75, \varepsilon=\pm 0.2$ and logic inputs of amplitude ± 0.2. This probability, P(logic), is the ratio of the number of correct logic outputs to the total number of runs. Each run samples over the four input sets (0,0), (0.1), (1,0), and (1,1), in different permutations. If the logic output, as obtained from $-x(t)$, matches the logic output in the truth table for all four input sets in the run, it is considered a success. When P(logic) is close to 1 the logic operation is obtained very reliably. It has been observed that the fundamental logic operation NAND (and, analogously, NOR) is realized, consistently, in an optimal band of moderate noise. The remarkable thing here, then, is that these stable logic operations are only realized (for subthreshold input signals) in the presence of noise. More specifically, *in relatively wide windows of moderate noise, the system yields logic operations with near certain probability* i.e., $P(\text{logic})\approx 1$; in this sense, the gate is quite robust to background fluctuations.

It is clear that (perhaps, somewhat counter intuitively) noise plays a constructive role in obtaining a large, robust, asymmetric response to input signals, i.e., different (and distinct) levels of input pulses yield 0/1 outputs, determined by the system being in either one of the two widely separated wells. This kind of response is necessary for logic operations, as it allows one to consistently map different distinct inputs to a binary output. Such mappings can be obtained, in principle, for any multiple-input logic operation through an appropriate choice of parameters.

As the value of the bias ε changes (keeping the nonlinearity and noise level fixed), it is observed that the response of the system switches from NOR to NAND logic, or vice versa. The important point is that changing ε changes the symmetry of the potential wells, and leads to different logical responses. It should be underscored that while the logic responses are switched by changing the nonlinearity or the bias, the desired output is obtained only for optimal noise intensities (Fig. 5), without which one would not be able to extract any significant consistent logic response. Significantly, one can *morph* between logic responses (NOR/OR to NAND/AND) by simply adjusting the dc input signal ε. Note that the effect of parametric perturbations (usually manifested as multiplicative or state-dependent noise) can be easily studied with this setup.

In summary, we are able to obtain the most basic ingredients of general purpose hardware that has the potential for reconfigurability. Another advantage of the present circuit is that it can be realized with a set of single-electron-transistor based inverters[5] so that one can further test the LSR paradigm in nanoelectronic devices.

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[1]A. R. Bulsara and L. Gammaitoni Phys. Today **49**(3), 39 (1996); L. Gammaitoni, P. Hanggi, P. Jung, and F. Marchesoni, Rev. Mod. Phys. **70**, 223 (1998).
[2]K. Murali, S. Sinha, W. Ditto, and A. Bulsara, Phys. Rev. Lett. **102**, 104101 (2009).
[3]M. M. Mano, *Computer System Architecture* (Prentice Hall, India, 1993).
[4]K. O'Donoghue, M. Kennedy, P. Forbes, M. Qu, and S. Jones, Int. J. Bifurcation Chaos Appl. Sci. Eng. **15**, 2959 (2005).
[5]G. Gandhi, T. Roska, A. Csurgay, T. Oya, T. Asai, and Y. Amemiya, Chaos, Solitons Fractals **32**, 855 (2007).