Device Scaling Effects on Hot-Carrier Induced Interface and Oxide-Trapped Charge Distributions in MOSFET's

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***Abstract*—The influence of channel length and oxide thickness on the hot-carrier induced interface (N_{it}) and oxide (N_{ot}) trap profiles is studied in n-channel LDD MOSFET's using a novel charge pumping (CP) technique. The technique directly provides separate N_{it} and N_{ot} profiles without using simulation, iteration or neutralization, and has better immunity from measurement noise by avoiding numerical differentiation of data. The N_{it} and N_{ot} profiles obtained under a variety of stress conditions show well-defined trends with the variation in device dimensions. The N_{it} generation has been found to be the dominant damage mode for devices having thinner oxides and shorter channel lengths. Both the peak and spread of the N_{it} profiles have been found to affect the transconductance degradation, observed over different channel lengths and oxide thicknesses. Results are presented which provide useful insight into the effect of device scaling on the hot-carrier degradation process.**

***Index Terms*—Channel length and oxide thickness dependence, charge pumping, hot-carrier effect, MOSFET, spatial profiling of damage.**

I. Introduction

With the aggressive reduction of MOSFET dimensions into the deep submicrometer regime, hot-carrier degradation (HCD) is becoming an important reliability issue. HCD results from heating and subsequent injection of carriers into the gate oxide, which results in a localized and nonuniform buildup of interface states (N_{it}) and oxide charges (N_{ot}) near the drain junction of the transistor. The generated defects produce threshold voltage shift, transconductance degradation, drain current reduction, etc., and eventually lead to device failure [1]–[4]. It is well known that HCD is a strong function of the internal electric field distributions of the MOSFET. While the lateral electric field near the drain junction is responsible for carrier heating and avalanche (monitored by substrate current), the transverse electric field influences carrier injection into the gate oxide (monitored by gate current) [4]–[8]. The reduction of channel length and oxide thickness of the transistor affects the internal electric field distributions and hence the carrier heating and injection processes. The damage creation and the resulting device degradation thus become a strong function of device dimensions and therefore merit attention.

Over the years, several attempts have been made to understand the effects of MOSFET scaling on HCD. It has been found that the reduction of MOSFET channel length increases the carrier heating process [9], [10]. Moreover, due to nonscaling of the region of the channel damaged by hot carriers, a relatively larger fraction of the channel gets affected for smaller channel lengths [11], [12]. Both these effects have a stronger impact on device characteristics and hence the degradation has been found to worsen with reduction in channel length [3], [4], [9]–[12]. With the reduction in oxide thickness, lesser degradation in terms of charge trapping (as measured using threshold voltage shift) has been reported [3], [13]–[18]. This can be attributed to reduced volume available for charge trapping [19] and tunneling of carriers from the oxide into the gate and substrate [20], [21]. On the other hand, enhanced carrier heating and avalanche (as measured using substrate current) was reported at lower oxide thicknesses [16]–[18]. Though in simple terms it means enhanced interface-trap generation [17], the transconductance degradation however has been found to be lesser for MOSFET's having thinner gate oxides [16]–[18], an observation which deserves close attention. Most of the work reported so far on the effects of MOSFET scaling on HCD has been performed using indirect methods, such as monitoring substrate and gate current (to estimate damage generation) and correlating it to the drain current degradation. However, due to the localized and nonuniform nature of hot carrier damage, it would be very useful to directly obtain the damage profiles and correlate these to drain current degradation in order to correctly understand and model the influence of MOSFET channel length and oxide thickness on HCD. This is the focus of this paper.

In order to obtain the spatial distribution of N_{it} and/or N_{ot} created during hot-carrier stress, different charge pumping (CP) based methods have been employed in the literature [22]–[30]. The simulation-based methods [22]–[26] are unsatisfactory due to the requirement of the knowledge of exact device structure and doping profiles. The direct methods either need separate neutralization steps and are complex in nature [27], [28] or need iterative numerical differentiation susceptible to measurement noise [29]. Moreover, it has recently been shown [31] that the methods [27]–[30] furnish incorrect spatial position of the damage profiles. To overcome the existing difficulties, we have recently proposed a new method [32] which does not require computer simulation, iteration or neutralization, is more

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immune to measurement noise (by avoiding experimental data differentiation), and provides an accurate distribution of N_{it} and N_{ot} created during hot-carrier stress. The new method has been successfully employed [33] to determine the time evolution of N_{it} and N_{ot} profiles in n-channel LDD MOSFET's, subjected to hot-carrier stress at different bias conditions.

This paper describes the application of the new CP method to determine the influence of device dimensions on hot-carrier damage creation in n-channel LDD MOSFET's. We have obtained, for the first time, a unique comprehensive set of data of the N_{it} and N_{ot} spatial profiles along the channel over a range of channel lengths and oxide thicknesses. The magnitude and spread of the damage profiles show well-defined trends with variation in device dimensions. The possible physical mechanisms responsible for such trends are discussed. Finally, the damage distribution is correlated to the device degradation obtained from drain current measurements. We have found that the N_{it} generation and the resulting transconductance degradation become the dominant degradation mode for devices having smaller channel lengths and oxide thicknesses. The transconductance degradation correlates well with the magnitude and spread of the generated N_{it} profiles, and has similar trends with the variation in device dimensions.

In Section II of this paper, the procedure of the new CP technique is briefly described. A fuller account has been presented elsewhere [32], where the correctness, reliability and robustness of the technique are also demonstrated. Results are presented and discussed in Section III, followed by conclusions in Section IV.

II. Experimental Technique

In charge pumping, the gate of the MOSFET is driven from accumulation to inversion and back using a trapezoidal waveform. The substrate is shorted to ground. The dc current (I_{cp}) arising out of electron-hole recombination at the interface states is measured at the source and drain, as shown in Fig. 1. The CP measurements are performed in two ways. In the first case, the pulse top ($V_{\rm top}$) is fixed in inversion ($V_{\rm top} = V_{\rm top,\,max} = 1$ V) and the pulse base ($V_{\rm base}$) is varied. The pulse scans the local flatband voltage (V_{FB}) distribution and the resulting I_{cp}–$V_{\rm base}$ data are recorded. In the second case, the pulse base is fixed in accumulation ($V_{\rm base} = V_{\rm base,\,min} = -4$ V) and the pulse top is varied. The pulse scans the local threshold voltage (V_T) distribution and the resulting I_{cp}–$V_{\rm top}$ data are recorded (details of the gate pulsing scheme can be found in [23] and [25]). Prestress measurements are performed on transistors having different drawn gate length (L_d). Poststress measurements are performed on transistors subjected to hot-carrier stress.

The stress-induced incremental CP currents are given by [32]

$$\Delta I_{cp}(V_{\rm base}) = qfW \int_0^{y_{1,\,s}} \Delta N_{it}(y)\,dy \tag{1}$$

$$\Delta I_{cp}(V_{\rm top}) = qfW \int_{y_{1,\,s}}^{y_{m,\,s}} \Delta N_{it}(y)\,dy \tag{2}$$

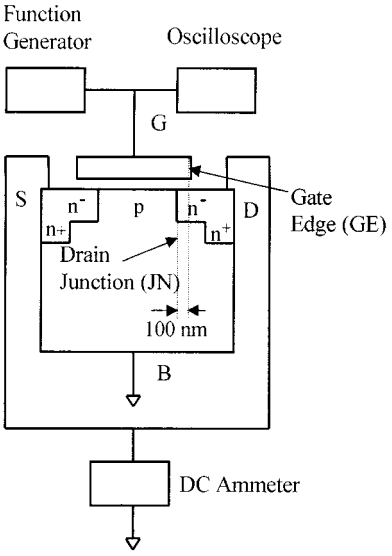

Fig. 1. Charge pumping setup along with the schematic diagram of the MOSFET used in the study showing drain junction (JN), gate-LDD overlap, and gate edge (GE).

$$\begin{aligned}&\Delta I_{cp}(V_{\rm base}) + \Delta I_{cp}(V_{\rm top})\\ &\quad = \Delta I_{cp,\,\max}(V_{\rm top\ max};\, V_{\rm base\ min})\\ &\quad = qfW \int_0^{y_{m,\,s}} \Delta N_{it}(y)\,dy\end{aligned} \tag{3}$$

where the origin is chosen at the center of the channel, q is the electronic charge, f is the frequency of the gate pulse, W is the device width, $\Delta N_{it}(y)$ is the generated interface-state density at y, and $y_{1,\,s}$ and $y_{m,\,s}$ are the CP edges in poststress and are defined by the relations

$$\begin{aligned}V_{FB,\,s}(y_{1,\,s}) &= V_{\rm base},\\ V_{T,\,s}(y_{1,\,s}) &= V_{\rm top}\end{aligned}$$

and

$$V_{FB,\,s}(y_{m,\,s}) = V_{\rm base,\,min}. \tag{4}$$

Here $V_{T,\,s}$ and $V_{FB,\,s}$ are the poststress local threshold and flatband voltage distributions along the channel, and are related to the corresponding prestress quantities V_T and V_{FB} by [32]

$$V_{T,\,s}(y) = V_T(y) - \frac{q\Delta N_{ot}(y)}{C_{ox}} + \frac{q\Delta N_{it}(y)}{2C_{ox}} \tag{5}$$

and

$$V_{FB,\,s}(y) = V_{FB}(y) - \frac{q\Delta N_{ot}(y)}{C_{ox}} - \frac{q\Delta N_{it}(y)}{2C_{ox}}. \tag{6}$$

Using (4)–(6) we write,

$$V_{\rm top} - V_{\rm base} = V_T(y_{1,\,s}) - V_{FB}(y_{1,\,s}) + \frac{q\Delta N_{it}(y_{1,\,s})}{C_{ox}} \tag{7}$$

where C_{ox} is the gate capacitance per unit area. For MOSFET's with thin gate oxides, the generated interface-state density pro-

file can be modeled by an analytically integrable function close to Gaussian in shape as [32]

$$\Delta N_{it}(y) = \frac{\Delta N_{it,p}}{\cosh^2 \alpha(y - y_p)} \tag{8}$$

where

- $\Delta N_{it,p}$ peak value of the damage;
- y_p position of the peak along the channel;
- α parameter whose reciprocal is a measure of the spatial spread of the damage.

Using (1), (2), (7), and (8) and assuming generated interface traps are negligible in the source half of the channel one obtains [32]

$$\Delta I_{cp}(V_{\text{base}}) = qfW \frac{\Delta N_{it,p}}{\alpha} [1 + \tanh \alpha(y_{1,s} - y_p)] \tag{9}$$

$$\Delta I_{cp,\max}(V_{\text{top,max}};\, V_{\text{base,min}}) = qfW \frac{\Delta N_{it,p}}{\alpha} [1+\beta] \tag{10}$$

$$y_{1,s} = y_{m,s} - \frac{1}{2\alpha} \ln\left[\frac{2-(1+\beta)X}{1-\beta X}\right] \tag{11}$$

$$\beta = \tanh \alpha(y_{m,s} - y_p) \tag{12}$$

$$V_{\text{top}} - V_{\text{base}} = V_T(y_{1,s}) - V_{FB}(y_{1,s}) + \frac{q}{C_{ox}} \cdot \frac{\alpha \Delta I_{cp,\max}}{qfW} [2-(1+\beta)X]X \tag{13}$$

$$X = \frac{\Delta I_{cp}(V_{\text{base}})}{\Delta I_{cp,\max}(V_{\text{top,max}};\, V_{\text{base,min}})}. \tag{14}$$

For all V_{base} and hence ΔI_{cp} values in poststress, the corresponding V_{top} is obtained from (3). The determination of V_T, V_{FB}, and $y_{m,s}$ are discussed later. Equation (13) is fitted with the experimental $V_{\text{top}} - V_{\text{base}}$ versus $\Delta I_{cp}/\Delta I_{cp,\max}$ data and the parameters α and β are obtained. By obtaining $\Delta N_{it,p}$ from (10) and y_p from (12), the interface-trap profile is constructed using (8) and (11). The ΔN_{ot} profile is then constructed using either (5) or (6).

In prestress, by assuming a symmetric transistor, the varying pulse base and top level CP currents can be written as [32]

$$I_{cp}(V_{\text{base}}) = 2qfW\langle N_{it}(V_{\text{base}})\rangle \left[\frac{Ld}{2} - \Delta y_{1,v}\right] \tag{15}$$

and

$$I_{cp,\max} - I_{cp}(V_{\text{top}}) = 2qfW\langle N_{it}(V_{\text{top}})\rangle \left[\frac{Ld}{2} - \Delta y_{1,v}\right] \tag{16}$$

where

- $\Delta y_{1,v}$ is the zone excluded from CP process and is related to the CP edge ($y_{1,v}$) by the relation $y_{1,v} = L_d/2 - \Delta y_{1,v}$;
- L_d drawn gate length;
- $\langle N_{it}\rangle$ patial average of prestress interface-state density.

The plot of $I_{cp}(V_{\text{base}})$ and $I_{cp,\max} - I_{cp}(V_{\text{top}})$ versus L_d is fitted with a straight line whose intercept gives $\Delta y_{1,v}$ and hence the CP edge $y_{1,v}$ for a given V_{base} and V_{top} value in prestress. The process is repeated for all V_{base} and V_{top} values and using the relation $V_T(y_{1,v}) = V_{\text{top}}$ and $V_{FB}(y_{1,v}) = V_{\text{base}}$, the prestress $V_T - y$ and $V_{FB} - y$ relations are obtained. Assuming negligible damage creation at $y_{m,s}$ (deep inside the channel-LDD junction), $y_{m,s}$ is obtained from the condition $y_{m,s} = y_{m,v}$ and $V_{FB}(y_{m,v}) = V_{\text{base,min}}$ [32]. For a fuller description of the technique as well as its experimental validation, the reader is referred to [32].

III. Results and Discussion

Charge pumping measurements using the method discussed above were carried out on submicrometer LDD MOSFET's as shown in Fig. 1. The gate of the MOSFET is pulsed using a trapezoidal waveform obtained from an HP33120A function generator. The charge pumping current is measured at the source and drain using a Keithley 617 electrometer, preceded by an LC lowpass filter. The substrate is shorted to ground. Measurements were performed using trapezoidal gate pulses having a frequency of 1 MHz with rise and fall time of 250 ns. For the varying base-level measurements, the pulse top was fixed at 1 V. For the varying top-level measurements, the pulse base was fixed at -4 V.

Experiments were performed using isolated LDD n-channel MOSFET's having a gate-LDD overlap of 100 nm as shown in Fig. 1. The channel length dependence studies were performed on devices having oxide thickness (T_{ox}) of 11 nm. The oxide thickness dependence studies were performed on devices having effective channel length (L_{eff}) of 0.3 μm. All the devices have a gate width of 10 μm. The threshold voltages (as measured from transfer characteristics at $V_D = 0.1$ V) for the devices having $T_{ox} = 11$ nm are 1.1, 0.81, 0.75, and 0.71 V, respectively, for $L_{\text{eff}} = 0.8$, 0.4, 0.3, and 0.25 μm, and for the devices having $L_{\text{eff}} = 0.3$ μm are 0.92, 0.75, 0.68, and 0.51 V, respectively, for $T_{ox} = 13$, 11, 9, and 5 nm. The prestress N_{it} of the devices is about 10^{10} (cm^{-2}) in the center of the channel, and increases by a factor of two to three toward the source and drain junctions. The stressing at different gate and drain voltages are performed on different transistors located on different (but adjacent) dies in the wafer. The length dependence studies are performed on devices on the same wafer, while the oxide thickness dependence studies are performed on devices on different wafers, processed identically but for the oxide thickness. We have found about a 10% variation in prestress charge pumping current measured on devices having identical structures but located at different parts of the wafer. However, for identical stress conditions, we have found almost identical incremental charge pumping current measured on identical devices. Since our analysis is based on the incremental charge pumping current, the small variations in charge pumping characteristics across the wafer do not affect our analysis.

A. Spatial Distribution of Interface Traps and Oxide Trapped Charges

Figs. 2–5 show the stress-induced ΔN_{it} and ΔN_{ot} profiles along the channel for transistors having different channel lengths (Figs. 2 and 3) and oxide thicknesses (Figs. 4 and 5).

The origin is now chosen at the channel-LDD junction. The stressing was done at $V_D = 5$ V for 100 s. The ΔN_{it} profiles of Figs. 2 and 4 are shown for stressing at $V_G = 2.5$ V, which also happens to be the condition for maximum substrate current. The ΔN_{ot} profiles of Figs. 3 and 5 are shown for stressing at $V_G = 1.2$ and 4.25 V. The stress biases were kept constant over channel lengths and oxide thicknesses to study the worst case damage condition. For all the channel lengths and oxide thicknesses used in this study, hole trapping ($\Delta N_{ot,h}$) is observed for stressing at $V_G = 1.2$ V, while electron trapping ($\Delta N_{ot,e}$) is observed at $V_G = 4.25$ V. No significant charge trapping is observed for stressing at $V_G = 2.5$ V [29], [33]. Maximum N_{it} generation takes place at $V_G = 2.5$ V. For stressing at $V_G = 1.2$ and 4.25 V, N_{it} is generated in lesser amount (not shown), the minimum being at $V_G = 4.25$ V (as also reported in [2], [3], [29], and [33]). The peak of the $\Delta N_{ot,h}$ profile is situated near the channel-LDD junction, while that of the $\Delta N_{ot,e}$ profile is inside the gate-LDD overlap region. The peak of the ΔN_{it} profile for stressing at $V_G = 2.5$ V is also observed in the gate-LDD overlap region. Using device simulations, it has been shown earlier [33] that the locations of the trapped charges and generated interface states for different bias conditions depend on the internal electric field distribution.

As shown in Figs. 2 and 3, with the reduction of MOSFET channel length, the ΔN_{it} and ΔN_{ot} distributions increase mostly in magnitude. The spread of the ΔN_{it} distribution increases by a little amount, while the spread of $\Delta N_{ot,h}$ and $\Delta N_{ot,e}$ distributions does not show any appreciable increase. The peak magnitude of ΔN_{it} distribution increases drastically for decreasing L_{eff}, compared to the increase in the peak magnitude of ΔN_{ot} profiles. As the oxide thickness of the transistor is reduced, the ΔN_{it} profiles increase in magnitude but decrease in spread, see Fig. 4. On the other hand, the ΔN_{ot} profiles decrease both in magnitude and in spread, and for $T_{ox} = 5$ nm, we observe hardly any charge trapping, see Fig. 5. Therefore, it is evident that with the reduction in device dimensions, the hot-carrier induced charge trapping will be insignificant and N_{it} generation will become the dominant degradation mode [3]. We have found identical L_{eff} and T_{ox} dependent trends of N_{it} generation for stressing at $V_G = 1.2$ and 4.25 V (not shown).

B. Physical Explanation of the Effect of Device Scaling on Damage Profiles

The observed L_{eff} and T_{ox} dependence of the ΔN_{it} profiles can be explained as follows. We refer to the trapped-hole recombination model [34], where the simultaneous presence of both hot electrons and hot holes are required in the oxide for the generation of interface traps. The increase in ΔN_{it} profiles for lower L_{eff} can be attributed to the increased lateral electric field (E_{lat}) and the drain current (I_D), which result in increased carrier heating and avalanche [3], [4], [9], [10]. However, device simulations with MINIMOS 6.0 show that the length of the velocity-saturated region (where E_{lat} is higher) remains almost the same with the reduction of L_{eff}. Therefore, with decreasing L_{eff}, injection of hot electrons and holes takes place almost over the same area, and though the magnitude of the ΔN_{it} profiles increases drastically, not much increase is observed in its spread

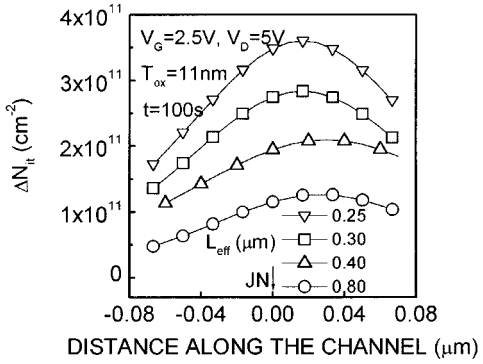

Fig. 2. Interface-state density (ΔN_{it}) profiles along the channel as a function of channel length. Stressing was done at $V_G = 2.5$ V, $V_D = 5$ V, for 100 s. The origin is chosen at the drain junction (JN), and the gate edge (GE) is at 0.1 μm.

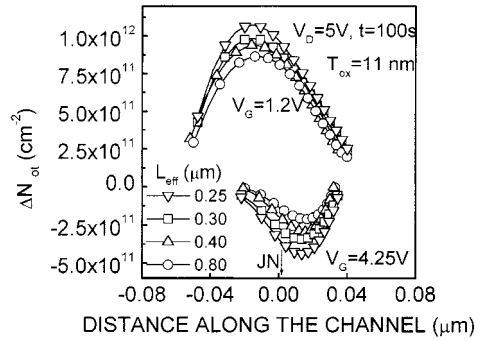

Fig. 3. Oxide trapped charge density (ΔN_{ot}) profiles along the channel as a function of channel length. Stressing was done at $V_G = 1.2$ and 4.25 V, $V_D = 5$ V, for 100 s. The origin is chosen at the drain junction (JN), and the gate edge is at 0.1 μm. Electron trapping is shown in the negative scale.

(see Fig. 2). With the reduction of T_{ox}, increased avalanching is observed (due to increased E_{lat}) as measured using substrate current [16]–[18] (also shown later). Furthermore, the higher transverse field aids in the carrier injection process. However, the zone inside the oxide where the electric field lines both originate and terminate at the substrate (close to the point where the transverse electric field changes sign), gets reduced in spread due to stronger transverse fields. Note that the two-dimensional (2-D) field distribution in this zone is responsible for lateral spreading of injected carriers inside the oxide [7]. Therefore for thinner T_{ox}, larger carrier injection takes place, but the injected carriers are confined to a narrow zone and cannot spread out, and the ΔN_{it} profiles get thinner in spread but larger in magnitude (see Fig. 4). This effect has important consequences for mobility degradation as discussed later.

We now explain the observed L_{eff} and T_{ox} dependence of the ΔN_{ot} profiles. Hole trapping is an efficient process due to large capture cross-section of the hole traps and low hole mobility in the oxide. So, all the existing hole traps are rapidly filled during the initial period of stressing, for stressing times as low as 10 s [33], which inhibits further hole trapping. Therefore, the $\Delta N_{ot,h}$ profiles do not increase significantly with reduction in L_{eff} (see Fig. 3). On the other hand, electron trapping takes place at high V_G values where the transverse electric field in the oxide is also higher, which results in field assisted detrapping of trapped electrons. This limits electron trapping, and the $\Delta N_{ot,e}$ profiles do not increase significantly with the reduction in L_{eff}

(see Fig. 3). For thinner T_{ox}, the existing oxide traps are less in number. Though carrier injection is enhanced for thinner oxides (due to higher transverse electric field), the tunneling of trapped carriers from regions close to the channel and gate interfaces results in lesser permanent charge trapping. These effects result in lesser ΔN_{ot} generation as T_{ox} is reduced (see Fig. 5) [19]–[21]. However, their exists a finite possibility that the trapped oxide charges were released during the CP measurements for thinner oxides, which may also be partially responsible for lower N_{ot} for smaller T_{ox}.

We next study the effect of ΔN_{it} profiles on transconductance (g_m) degradation over different channel lengths and oxide thicknesses. Experiments were performed for two different stress conditions. In the first case, the stress biases were kept constant over channel lengths and oxide thicknesses to study the worst-case damage condition. In this case, both the peak and the spread of the ΔN_{it} profiles changes with the reduction in device dimensions, and the corresponding g_m degradation is studied. In the second case, the stress V_D was adjusted over channel lengths and oxide thicknesses for identical substrate current (I_{sub}) during stress. Since I_{sub} measures avalanching near the drain junction, the peak of the ΔN_{it} profiles remain constant, while its spread is varied. Therefore, this experiment is useful to separately study the effect of damage spread on g_m degradation, over different channel length and oxide thickness of the device. Results of these two types of stress are described in the next two sections.

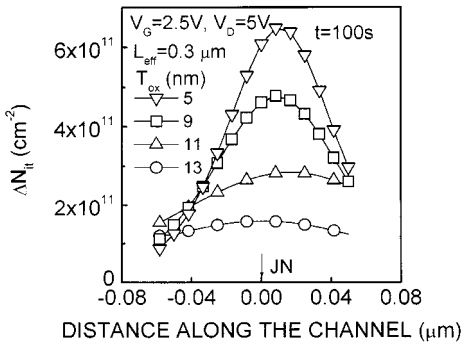

Fig. 4. Interface-state density (ΔN_{it}) profiles along the channel as a function of oxide thickness. Stressing was done at $V_G = 2.5$ V, $V_D = 5$ V, for 100 s. The origin is chosen at the drain junction (JN), and the gate edge (GE) is at 0.1 μm.

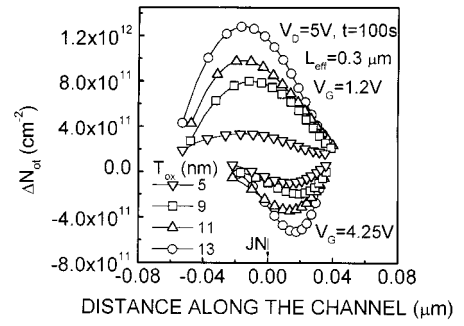

Fig. 5. Oxide trapped charge density (ΔN_{ot}) profiles along the channel as a function of oxide thickness. Stressing was done at $V_G = 1.2$ and 4.25 V, $V_D = 5$ V, for 100 s. The origin is chosen at the drain junction (JN), and the gate edge is at 0.1 μm. Electron trapping is shown in the negative scale.

C. Transconductance Degradation Under Constant Bias Stress Experiments

Figs. 6 and 7 show the interface-state density peak ($\Delta N_{it,p}$), the measured substrate current during stress (I_{sub}), the normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$) (left y axis), the spread of interface trap profile ($\Delta\sigma$) and the incremental CP current (ΔI_{cp}) (right y axis) as a function of channel length (Fig. 6) and oxide thickness (Fig. 7), measured from constant bias stress experiments. The stressing was performed at $V_G = 2.5$ V, $V_D = 5$ V for 100 s, for all the channel lengths and oxide thicknesses used in the study. The damage spread $\Delta\sigma$ is defined as the length of the channel where the magnitude of the generated N_{it} is greater than 5×10^{10} (cm^{-2}) [33]. Note that this choice of N_{it} to define the damage spread is somewhat arbitrary and a different cut-off value would result in a different value of $\Delta\sigma$. However we have found that the trends in $\Delta\sigma$ remains independent of the choice of the cut-off value. The transconductance (peak value) is calculated from the $I_D - V_G$ characteristics measured at $V_D = 0.1$ V, both before and after stress.

As can be seen from Figs. 6 and 7, with the reduction in both L_{eff} and T_{ox}, an increase is observed in the measured I_{sub} during stress. Therefore, an increase is also observed in the peak value of the ΔN_{it} profiles. With the reduction in L_{eff} (from 0.8 to 0.3 μm), I_{sub} and $\Delta N_{it,p}$ are increased by a factor of 2.8 and 2.6, respectively, close to each other. With the reduction in T_{ox} (from 13 to 5 nm), I_{sub} and $\Delta N_{it,p}$ are increased by a factor of 2.5 and 3.2, respectively. The higher $N_{it,p}$ generation (compared to increase in I_{sub}) for thinner oxides can be attributed to the higher transverse electric field (thereby higher carrier injection) for such devices. Contrary to $\Delta N_{it,p}$, $\Delta\sigma$ shows opposing trends with variation in device dimensions. With the reduction in L_{eff}, $\Delta\sigma$ increases by a factor of 1.2. On the other hand, with the reduction in T_{ox}, $\Delta\sigma$ reduces by a factor of 1.5. Hence, it is evident that $\Delta\sigma$ does not correlate with the I_{sub} trends. Furthermore, note that ΔI_{cp} is a measure of total N_{it} generation and is proportional to $\Delta N_{it,p} \times \Delta\sigma$. Therefore, a large increase in ΔI_{cp} (a factor of 3.5) is observed as L_{eff} is reduced, while with the reduction in T_{ox}, ΔI_{cp} is increased only by a factor of 1.8.

The observed trends in $\Delta N_{it,p}$ and $\Delta\sigma$ are also reflected in the normalized peak Δg_m. For the first time, thanks to the availability of spatial profiles, we are able to correlate Δg_m dependence on L_{eff} and T_{ox} with the individual variation of $\Delta N_{it,p}$ and $\Delta\sigma$. Since both $\Delta N_{it,p}$ and $\Delta\sigma$ increase with the reduction in L_{eff} (note that the fraction of the degraded channel is increased by a factor of 4.8), Δg_m is increased by a factor of 5.4, much larger than the individual increase in $\Delta N_{it,p}$ and $\Delta\sigma$ (see Fig. 6). Similar L_{eff} dependence of g_m degradation have been reported earlier [9]–[12]. On the other hand, $\Delta N_{it,p}$ increases and $\Delta\sigma$ decreases with the reduction in T_{ox}, so no significant g_m degradation (or improvement) is observed (see Fig. 7). Note that our result is not in full agreement to those previously published [16]–[18], where lesser g_m degradation is reported (despite higher I_{sub}) for thinner T_{ox}. However, it is important to note that despite higher I_{sub} for thinner T_{ox}, the reduction of the spread of ΔN_{it} profile is responsible for the observed trends

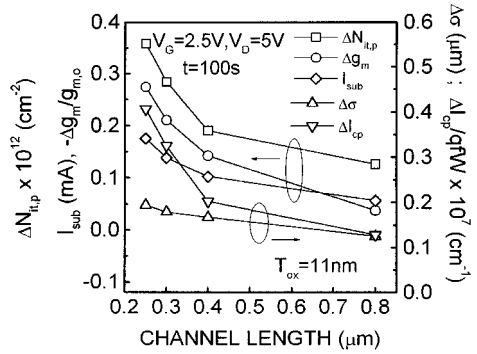

Fig. 6. Interface-state density peak ($\Delta N_{it,p}$), substrate current during stress (I_{sub}), normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$) (left y axis), interface-state density spread ($\Delta\sigma$), and incremental charge pumping current (ΔI_{cp}) (right y axis) as a function of channel length ($L_{\rm eff}$). Stressing was done at $V_G = 2.5$ V, $V_D = 5$ V for 100 s on a transistor having $T_{ox} = 11$ nm.

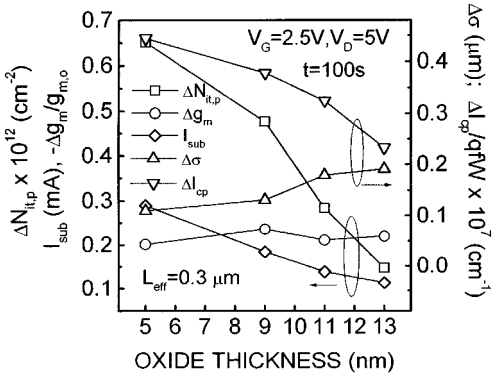

Fig. 7. Interface-state density peak ($\Delta N_{it,p}$), substrate current during stress (I_{sub}), normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$) (left y axis), interface-state density spread ($\Delta\sigma$), and incremental charge pumping current (ΔI_{cp}) (right y axis) as a function of oxide thickness (T_{ox}). Stressing was done at $V_G = 2.5$ V, $V_D = 5$ V for 100 s on a transistor having $L_{\rm eff} = 0.3$ μm.

in g_m degradation. Therefore, it is evident that the g_m degradation is affected not only by the peak magnitude of the generated N_{it} profile, but also by the spread of the degraded channel. The effect of $\Delta\sigma$ on g_m degradation is elaborated further in the following discussion.

D. Transconductance Degradation Under Constant Substrate Current Stress Experiments

Figs. 8 and 9 show $\Delta N_{it,p}$, $\Delta\sigma$ (left y axis), $\Delta g_m/g_{m,o}$ and the fraction of the degraded channel ($\Delta\sigma,\ f = \Delta\sigma/L_{\rm eff}$) (right y axis) as a function of channel length (Fig. 8) and oxide thickness (Fig. 9), measured from constant I_{sub} stress experiments. The stressing was performed at the $V_G = V_D/2$ condition for 100 s, and the stress V_D was suitably adjusted over channel lengths and oxide thicknesses to obtain $I_{sub} = 130$ μA during stress.

As can be seen from Figs. 8 and 9, since V_D is reduced and I_{sub} (hence, avalanching) is held constant with the reduction in $L_{\rm eff}$ and T_{ox}, no significant increase is observed in $\Delta N_{it,p}$. (The slight increase in $\Delta N_{it,p}$ with lower T_{ox} can be attributed to higher injection in thinner oxides). However, the percentage of the degraded channel ($\Delta\sigma,\ f$) still increases by a factor of 2.5

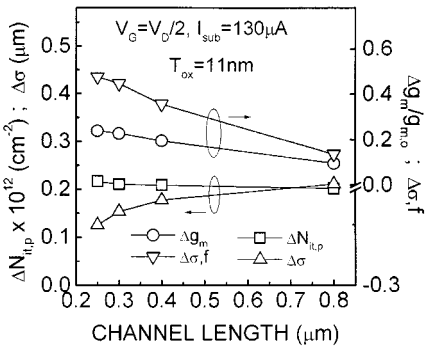

Fig. 8. Interface-state density peak ($\Delta N_{it,p}$), spread ($\Delta\sigma$) (left y axis), normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$), and fraction of the degraded channel ($\Delta\sigma,\ f$) (right y axis) as a function of channel length ($L_{\rm eff}$). Stressing was done at $V_G = V_D/2$, $I_{sub} = 130$ μA for 100 s on a transistor having $T_{ox} = 11$ nm.

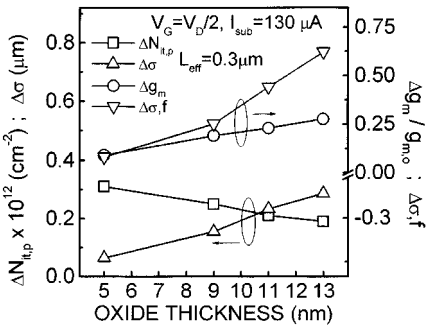

Fig. 9. Interface-state density peak ($\Delta N_{it,p}$), spread ($\Delta\sigma$) (left y axis), normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$), and fraction of the degraded channel ($\Delta\sigma,\ f$) (right y axis) as a function of oxide thickness (T_{ox}). Stressing was done at $V_G = V_D/2$, $I_{sub} = 130$ μA for 100 s on a transistor having $L_{\rm eff} = 0.3$ μm.

with the reduction in $L_{\rm eff}$, and hence an increase is observed in Δg_m (a factor of 2.3, see Fig. 8). On the other hand, with the reduction in T_{ox}, $\Delta\sigma,\ f$ is reduced by a factor of 3.5, and hence a decrease is observed in Δg_m (by a factor of 2.9). The lower decrease in Δg_m (compared to $\Delta\sigma,\ f$) can be attributed to the slight increase in $\Delta N_{it,p}$ as discussed above. This again verifies unambiguously the fact that the spread of the degraded channel is also responsible for g_m degradation, not just $\Delta N_{it,p}$.

IV. Conclusion

To summarize, a novel charge pumping technique is employed to obtain the spatial profiles of interface (N_{it}) and oxide trapped-charge (N_{ot}) in hot-carrier stressed MOSFET's. We have obtained a unique comprehensive set of data on damage distributions for different stress biases, over different channel length ($L_{\rm eff}$) and oxide thickness (T_{ox}) of the device. It has been found that hole trapping, N_{it} generation and electron trapping are the dominant degradation modes, respectively, for stressing at low, medium and high gate biases. With the reduction in $L_{\rm eff}$, the ΔN_{it} profiles increase both in magnitude and in spread, the increase in magnitude being much larger compared to the increase in spread. Only the peak of the ΔN_{ot} profile increases with decreased $L_{\rm eff}$, though the increase is much less compared to the corresponding increase in the ΔN_{it} peak. With the reduction in T_{ox}, the ΔN_{it} profiles

increase in magnitude but decrease in spread, while the ΔN_{ot} profiles decrease both in magnitude and in spread. The possible mechanisms responsible for such trends are discussed. It has been shown that for devices having smaller channel length and thinner gate oxide, N_{ot} generation is insignificant, and the N_{it} generation (at medium gate bias) becomes the dominant degradation mode. The observed peak g_m degradation is found to be dependent on both the peak magnitude and spread of the generated N_{it} profiles, and follows similar trends with the variation in channel length and oxide thickness. This study therefore provides fresh insight into the effect of device scaling on the hot-carrier degradation process.

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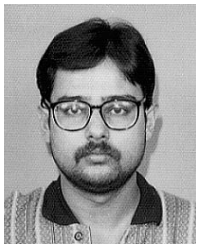

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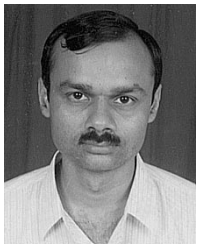

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