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ON THE SYSTEM AND ENGINEERING DESIGN OF THE GENERAL PURPOSE ELECTRONIC DIGITAL COMPUTER AT T.I.F.R.

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1. Introduction

Since 1955, the Computer Section of the Tata Institute of Fundamental Research has been engaged in the development and construction of a large-scale electronic digital computer for doing scientific computations. As a preliminary to this, a pilot digital calculator was designed and completed in September 1956 and was kept in operation for about a year.[1] The design of the full-scale machine was started early in 1957 and its final assembly completed in February 1959. Unfortunately, owing to the lack of air-conditioning facilities, the work had to be suspended till almost the end of 1959. The actual testing was begun in mid-November 1959 with an auxiliary air-conditioning system and the computer was commissioned for routine work in the third week of February 1960. This paper describes briefly the main features of the system and engineering design of this digital computer. In a companion paper, some aspects of the circuitry will be dealt with.

The T.I.F.R. computer is a parallel, binary, asynchronous machine. It is controlled by a stored programme of single-address instructions and has a fast access ferrite-core memory consisting of 1,024 locations. The input to the computer is by means of a punched paper tape (5-hole commercial teletype tape) and the output can be either printed out directly or punched on a paper tape again.

Both in the system and engineering design, the principal emphasis has been on reliability of operation and ease in maintenance. With this in view, the logical circuit types have been kept to the minimum consistent with flexibility and the wired circuits were put through a rigid acceptance test to check their performance under extreme operating conditions. For rapid fault localization and servicing, a large part of the computer has been assembled

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in terms of functionally self-contained packaged units. Separate testing facilities have been set up for routine checking of these plug-in units.

The main computer assembly has 2,700 tubes (almost all of them double-triodes), 1,700 crystal diodes (germanium) and approximately 12,500 resistors. Since the computer is d.c. coupled throughout, few condensers are used and except in the case of two bias supplies, no circuit is transistorised. The total power consumption is about 18 K.W.

2. THE ARITHMETIC AND CONTROL LOGIC

In the T.I.F.R. computer, all the internal operations take place in the binary notation and numbers are stored in the main memory as signed binary fractions restricted to the range $(-1, 1)$. A number in its normal form consists of a sign (which is a 0 for positvie numbers and a 1 for negative numbers) followed by 39 binary digits (bits, for short) which give its absolute value as a binary fraction. The binary point is understood to be fixed immediately after the sign bit (*see* Text-Fig. 1). The complement form of a number is obtained by changing all its 1's to 0's and *vice-versa* ; the sign bit is left unaltered, however, in this process.

BINARY
POINT

SIGN | 2^{-1} | 2^{-2} ..... 2^{-37} 2^{-38} 2^{-39}
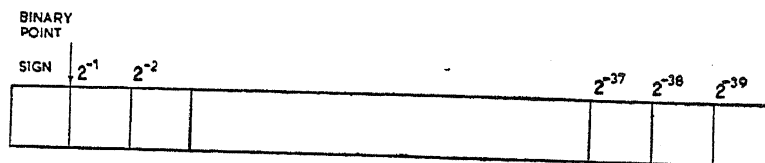
TEXT-FIG. 1. Number Representation (Binary Fraction).

A schematic diagram of the arithmetic unit is shown in Text-Fig. 2. It consists of an adder, a memory register and two (double rank) shift registers (the accumulator and MQ-register, respectively) and a pair of true/complement gates. The adder is of the fast logical type and incorporates in itself special carry by-pass facilities to speed up the carry propagation time.[2] These cut down the addition time to about one-third of what it would otherwise have been. The contents of the accumulator are presented to the adder either in the true or the complement form depending on whether the operation called for is addition (multiplication) or subtraction (division) respectively. In some cases the result of a subtraction needs to be recomplemented to obtain the number in its true form. To simplify this procedure, facilities have been built into the adder so that its output can be gated into the accumulator either in its true or complement form. Also the particular design of the adder used makes it especially simple to obtain the logical product of the adder inputs and this is taken advantage of in the Collate order.

The absolute value representation of numbers makes the multiplication and division logic very simple and straightforward. In both cases, the operation is carried out treating the numbers as positive quantities. The proper signs are written into the accumulator and MQ-register in the end. The incorporation of an extra bit, called the *Sense bit* (2^{-40} stage of MQ) is believed
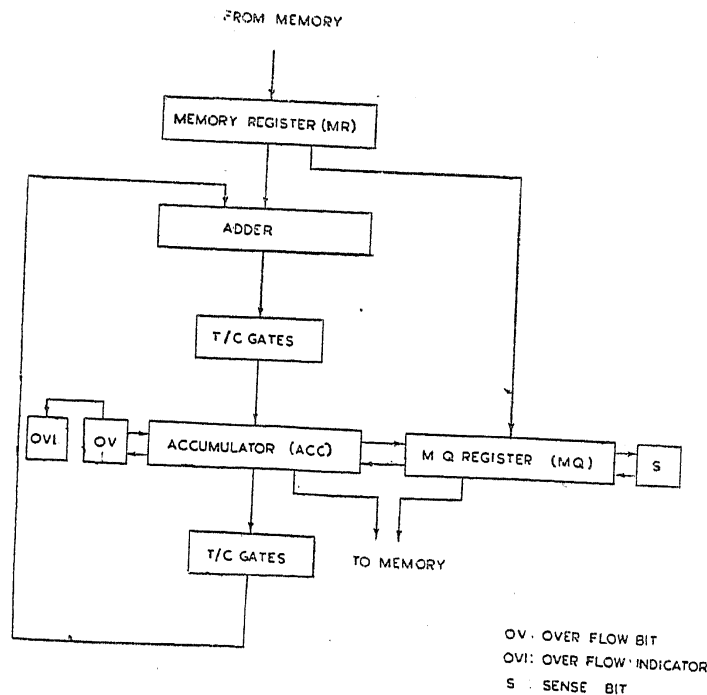

TEXT-FIG. 2. Schematic of Arithmetic Unit.

to be a unique feature of this computer. In multiplication, the discrimination for add-shift/shift is obtained from this sense bit rather than from Q^{-39} as is normally done. Similarly, in division the quotient bits are written into the sense bit rather than into Q^{-39}. Thus both multiplication and division involve 40 shifts (instead of the usual 39). This has the major advantage that normal division is unrounded (*i.e.*, is correct up to and *including* the 2^{-39} stage). It is expected that this feature will have special advantages in multiple precision work. In shift operations, the sense bit functions like an extension to the MQ-register on its right end.

All *proper* arithmetic operations should result in numbers which again fall within the range $(-1, 1)$. But there are no built-in checks to detect improper arithmetic operations. It is, in the main, the responsibility of the programmer to see that numbers are confined to the admissible range, by proper scaling, all the time. However, to help him in doing this, an extra bit, called the overflow bit, has been provided at the left end of the accumulator. In the case of a genuine overflow (*i.e.*, addition of numbers with the

same signs, or subtraction of numbers with opposite signs) it is fed into the overflow bit and an overflow indicator, OVI (which normally stays 0), is set to 1. This is not reset to 0 unless explicitly called for by the programmer. A "jump on overflow" order enables the programmer to make use of this information in variable scaling of numbers or in normalising in floating point arithmetic. Also, in ordinary shift operations, the overflow bit functions as an extension to the accumulator on the left and the OVI becomes operative when a 1 is shifted into the overflow bit.

A "round-off" order enables the accumulator content to be rounded off by adding a 1 or 0 to its least significant bit according as the MQ content is greater than or less than $\frac{1}{2}$.

As has already been mentioned, the T.I.F.R. computer is of the asynchronous, single address type. The details of its control logic are effectively determined by these two features. A coded instruction in the machine requires 20 bits for its specification: (the first 9 bits for its *order* part and last 11 bits for its *address* part). Because the word length in the memory is 40 bits, instructions are stored in pairs in each memory location. They are identified as the left-hand (L.H.I.) and right-hand (R.H.I.) instructions in that location (*see* Text-Fig. 3). A complete control cycle consists of 3 parts: (1) an *instruction cycle*, where a (next) pair of instructions is brought from the memory to the instruction register ; (2) an *execution cycle A*, where the left-hand instruction is executed and (3) an *execution cycle B* where the right-hand instruction is executed. The sequencing within the cycles is effected by means of 4-state sequencing units similar to the ones used in ORDVAC type machines.[3] The static control levels are obtained by partial decoding of the order bits of an instruction. As far as possible, the micro-operations are done in parallel so as to minimise the number of sequencing steps required.
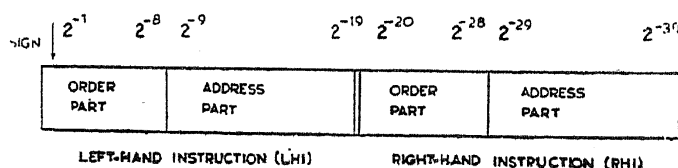
TEXT-FIG. 3. Allocation of bits in a pair of instructions.

One built-in B-register (of 11 bit length) is available for address modifications. The shift counter is also similar to the one used in ORDVAC but an improved gating logic has enabled its speed to be increased appreciably.[4]

In addition to the unconditional jump order, 6 types of conditional jump orders are available, *viz.*, jump if accumulator sign bit is 0/1 ; jump if MQ-sign bit is 0/1 ; jump if the overflow indicator is 0/1. In the case of the last order, the control resets the overflow indicator to 0.

Table I gives a summary of the order types and variants built into the computer.

TABLE I

Order types and their variants

	Type	Variants	
1. Arithmetic orders	Add	Hold Acc. Signed/Abs. Val.	Clear Acc. Signed/Abs. Val.
	Subtract	,,	,,
	Multiply Unround	,,	,,
	Multiply Round	,,	,,
	Divide	,,	,,
	Collate	,,	,,
	Round off	,,	,,
2. Shift orders ..	Shift Rt. Acc.	Hold Acc.	Clear Acc.
	Shift Lt. Acc.		
	Shift Rt. Acc.-MQ	,,	,,
	Shift Lt. Acc.-MQ	,,	,,
	Shift Lt. Acc.-MQ (also Q°)	,,	,,
3. Store orders ..	Store Acc.	Hold Acc-MQ	Clear Acc.
	Store LHA Acc.	,,	,,
	Store RHA Acc.	,,	,,
	Store LHA-RHA Acc.	,,	,,
	Store MQ	,,	,,
	Transfer to MQ	,,	,,
	Transfer to B-Reg.	,,	,,
4. Jump orders ..	If $A° = 0$	To LHI	To RHI
	If $A° = 1$	,,	,,
	If $Q° = 0$	,,	,,
	If $Q° = 1$	,,	,,
	If $OVI = 0$	,,	,,
	If $OVI = 1$	,,	,,
	Unconditional	,,	,,
5. Miscellaneous orders	Conditional Stop	Stop	
	Stop	..	
	Input	Tape/Drum	
	Output	Punch/CRT/Drum	
Operating Speed ..	Instruction cycle:	20 μ-sec.	
	Execution cycle— Add/subtract:	45 μ-sec.	
	Mult./Divide:	500 μ-sec.	
	Shift n:	$14 + 11\ n\ \mu$-sec.	

3. The Memory

The internal memory of the T.I.F.R. computer consists of a 3-dimensional ferrite-core matrix (made up of 40 planes), 40 output amplifiers, diode decoding nets for address selection and drive circuits for reading and writing. The matrix assembly was purchased from Mullard and Co., England. The read-rewrite logic is essentially the same as that described by Papian originally for the MIT computer.[6] Both amplitude and time discrimination (Strobing) is used at the output end to increase the signal/noise ratio. The read output is gated into a set of memory flip-flops which also function as the memory register of the arithmetic unit. The input to the memory can be either from the accumulator or the MQ-register. While storing from the accumulator, either the entire content of the register or only the address part (either the left-hand or right-hand address alone or both) can be written in. Except for the initiating trigger, the memory sequencing is completely independent of the rest of the computer control. The duration of a single memory read-write cycle is approximately 15 μ-seconds.

Provision has been made for incorporating a second core-matrix of equal capacity at a later stage thus doubling the internal store.

4. The Power Supply

The power requirements of a large-scale parallel electronic digital computer pose some severe problems normally not encountered in conventional electronic systems of a similar size. The power supply system, while large in capacity (usually of the order of 20 K.W.), has to be at the same time (1) very highly reliable and rugged ; (2) well stabilised for not only the usual line voltage fluctuations but for load switchings at very high repetition rates (calling for a response time of the order of a few μ-seconds on the part of the regulator for almost 0 to full-load switching) and (3) fully protected against partial failures by effectively fool-proof protective interlocks. The power supply for the T.I.F.R. computer has been designed and constructed to satisfy all the above requirements and has been under satisfactory operation for several months.

The input to the power supply is from 3-phase, 4 wire, 50 cycles, 230 volt mains with a nominal rating of 40 KVA. Two regulators are provided, one an electromechanical unit capable of handling up to 20 KVA and is intended principally for the tube heater supplies. The other is an electronic stabilizer for the high tension busbars in the computer.

The filament transformers are signle-phase units, each capable of supplying 200 amps. at 6·3 volts. 10 such transformers are used in all to supply the

heater power for the various units of the computer. A relay controlled system allows gradual application of filament voltages to the tubes and provides the necessary delay before the application of plate voltages.

The d.c. high tension levels used in the computer together with their full-load currents are as follows:

$$- 300 \text{ V} : 18 \text{ amps.}$$

$$- 150 \text{ V} : 4 \cdot 5 \text{ amps.}$$

$$+ 110 \text{ V} : 10 \text{ amps.}$$

$$+ 150 \text{ V} : 5 \text{ amps.}$$

$$+ 200 \text{ V} : 7 \text{ amps.}$$

$$+ 300 \text{ V} : 2 \text{ amps.}$$

These voltages are stabilised to within 1% for line voltage fluctuations and to within 2% for 0 to 100% load switching with a recovery time of the order of a few μ-seconds. The electronic regulator consists of grid controlled thyratrons used in a 3-phase half-wave circuit and a " stiff " filter with a large output capacitance (of the order of a few hundredths of a farad for each level) to provide the necessary recovery time. A specially developed pulse-shifting circuit fires the thyratrons.

5. ENGINEERING DESIGN

Figures 4 and 5 show an overall view of the computer assembly and power supply units. The main computer assembly is housed in a steel rack $18' \times 2\frac{1}{2}' 6'' \times 8'$ which has been fabricated out of modules of size $4' \times 2\frac{1}{2}' \times 8'$. Each module has a pair of steel doors (of size $2' \times 6'$) on either face to provide accessibility to the circuits. For ease in maintenance, single layer mounting has been adopted for the wired panels except in a few instances where a second layer has been wired on swing-out panels. The information flow is along the horizontal with the arithmetic unit in the centre flanked on either side by the control and the memory units. The bits in each functional unit occupy the modules from top to bottom. The lower $18''$ of the entire assembly house the filament transformers and some of the output capacitors while also serving as an air plenum for the forced-air-cooling system. Cool air (at approximately 20° C. and a total flow of 6,000 c.ft./min.) is fed into the computer at the two ends, channelled through the various modules and exhausted into the room from the top. Exhaust fans mounted along the length of the computer

on top help to maintain uniform distribution of the cold air inside the computer assembly.

The power unit is housed in two independent racks, one containing the contactors, a.c. regulators, variacs, transformers and output capacitors, and the other containing the thyratrons, pulse control units, control and voltage monitoring relays. The electronic circuitry is mounted on pull-out chassis to facilitate servicing.

6. Auxiliary Equipment

As has already been mentioned, the information input into the computer is by means of punched paper tapes and the output from the machine can again be either punched on tapes or directly printed out. Currently, commercial Olivetti Type T2Pr/T2CN reperforators and page printers are being used for this purpose. A Ferranti Mark II tape reader has been tried out but a much faster servo-controlled Potter Model 903 tape reader is in an advanced stage of testing and is expected to be available for use very soon. A high speed Creed Model 75 page printer/reperforator has also been acquired with a specially built-in code to facilitate direct binary to decimal conversion. This, together with the Potter tape reader, it is expected, will provide very adequate input-output facilities for the computer.

A manual control console has been set up to serve as a very flexible input/output/control unit to regulate and monitor the operation of the computer. Facilities are available for single shot operation; for slow external triggering at approximately one cycle per second and for manual sexadecimal input into the MQ-register with the help of a diode decoding net operated from a keyboard. Neon indicators enable visual monitoring of the contents of all the registers.

For routine maintenance checking and also for servicing of the various plug-in units used in the computer, a comprehensive test rack has been built. Detailed and systematic d.c. checking of the units can be carried out with great ease with the help of the test rack and complete test schedules have been worked out for each unit to systematise the test procedures.

A cathode ray tube (C.R.T.) display system has been developed to serve as an auxiliary output to the computer for fast analogue and digital display of both graphs and alpha-numeric symbols. A pilot version has already been built and successfully operated.[7] The more elaborate final unit is under assembly and is expected to be available for routine use in a few months' time.

Work on the development of a magnetic drum to serve as a large capacity back-up storage has been going on concurrently with the assembly of the main computer. The final specifications of the drum have been drawn up and the mechanical assembly is under fabrication. Logical design of the drum control and read-write circuits are being finalised. When this facility is made available, the total computer storage capacity will increase eight-fold.

7. OPERATIONAL EXPERIENCE

Since the completion of the computer assembly early in 1959, the various parts of the machine have been under operation for almost a year now. The operational and maintenance experience gained over this period indicate that with adequate *routine* maintenance, the computer should give reliable, trouble-free operation over long periods of time continuously. It has not been possible so far to collect systematic statistics of failure rates, of types of faults and of time lost in unscheduled servicing. However, it may be mentioned that in general the component failures have been remarkably few in number. Less than 5% of the tubes have had to be changed (and this mostly for loss in emission) and there have been resistance failures only in the case of 2 or 3 types of resistors.

Comprehensive test programmes have been designed to check each of the functional units under a variety of input-internal state configurations. These have proved to be of invaluable aid in fault location and in routine checking. By means of test programmes every single core in the memory matrix has been tested for reading and writing under the most adverse operating conditions.

It is proposed to operate the computer, at the first instance, on an 8-hour shift daily. The first 3 hours will be devoted to scheduled maintenance and the remaining 5 for useful computing. A programming manual has been prepared to assist machine users in programming their own problems.

8. SUMMARY

This paper gives a brief description of the system and engineering design of the general purpose electronic digital computer that has been developed and built in T.I.F.R., Bombay. This computer is a parallel, binary, asynchronous machine with a ferrite-core matrix fast memory of 1,024 words. The arithmetic is in the fixed point binary system with a number length of 40 bits. The computer incorporates one B-register for address modification and several other special features such as overflow indication, carry bypass, etc., Input-output is by means of punched paper tape. An auxiliary output in the form of a CRT display has been developed and a magnetic drum to serve as a back-up store is being designed.

9. ACKNOWLEDGMENTS

10. REFERENCES

1. "The Pilot Digital Calculator at T.I.F.R., Bombay," *The Digital Computer Newsletter,* January 1957.

2. Rao, P. V. S. and Basu, B. K. "A fast logical adder," *Tech. Report* (unpublished).

3. *ORDVAC Manual*—University of Illinois, 1952.

4. Basu, B. K. and Rao, P .V. S. "A modified gating logic to improve the speed of operation of double rank counters," *Proc. Ind. Acad. Sci.,* 1957, **46**, 354–59.

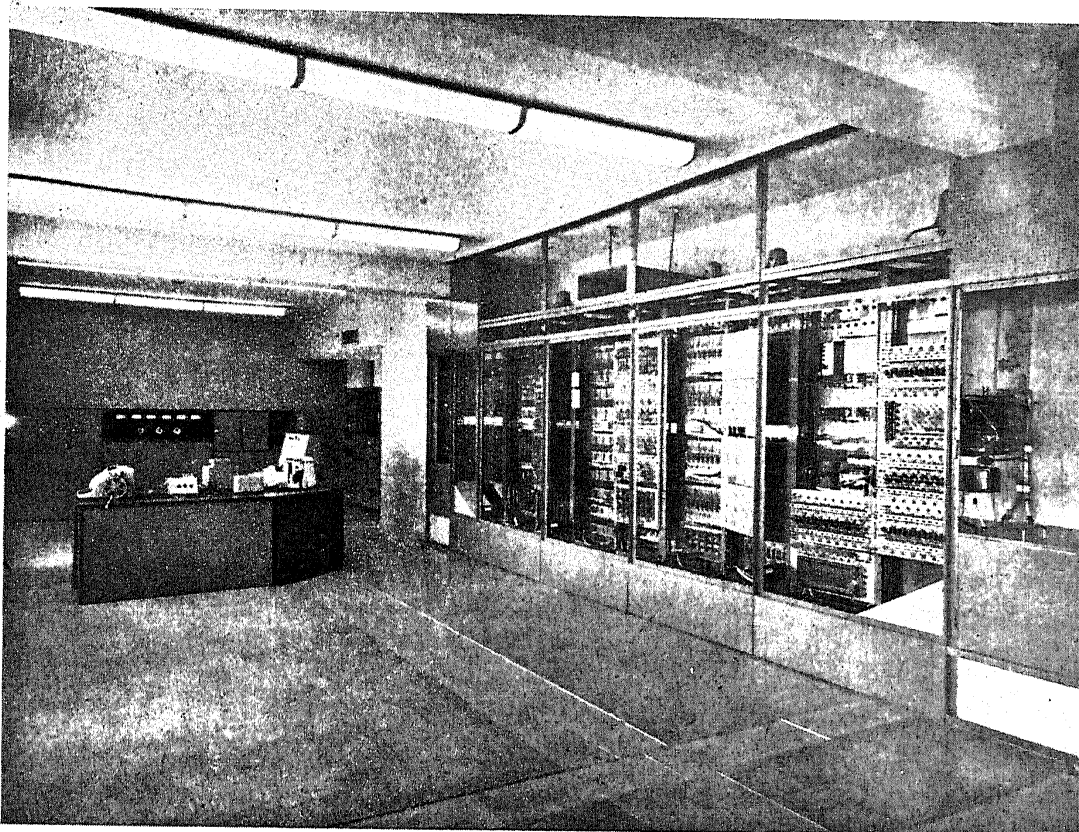5. ———— and Bakhru, K. "The input-output system of the T.I.F.R. computer," *Ibid.,* 1957, **45**, 231–39.

FIG. 4. The Computer Assembly (with doors removed) showing the Manual Console and the power supply units.
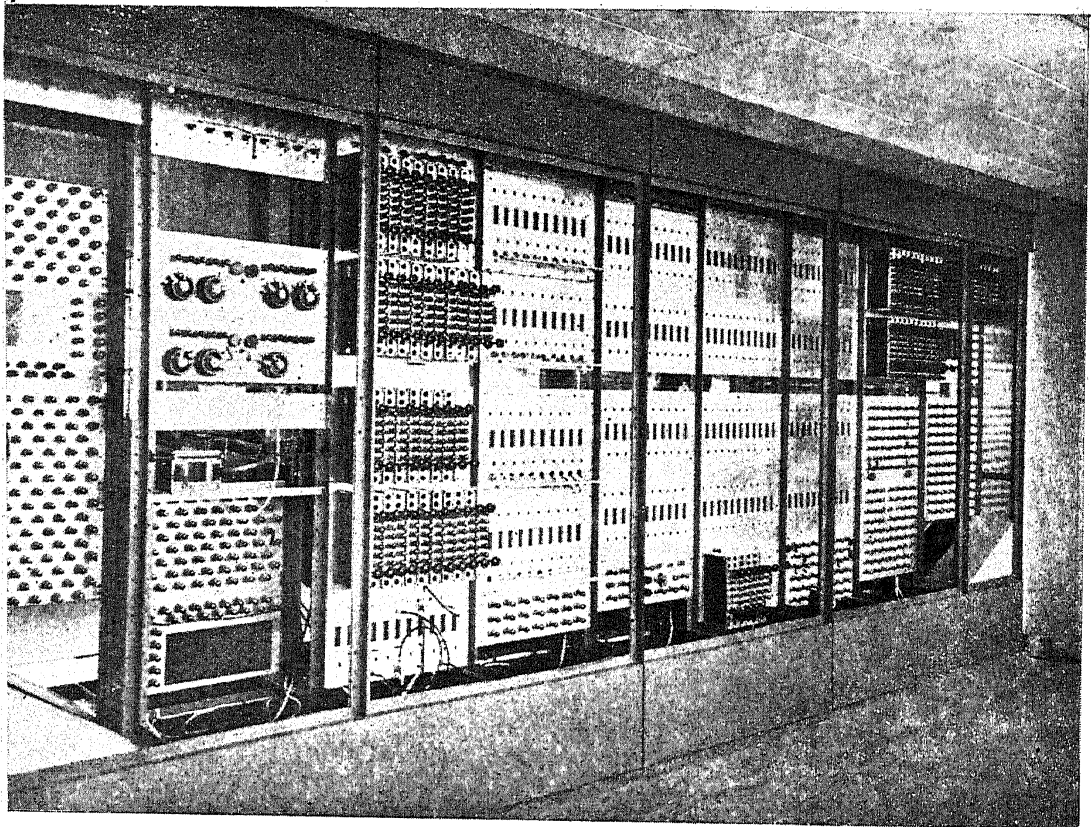
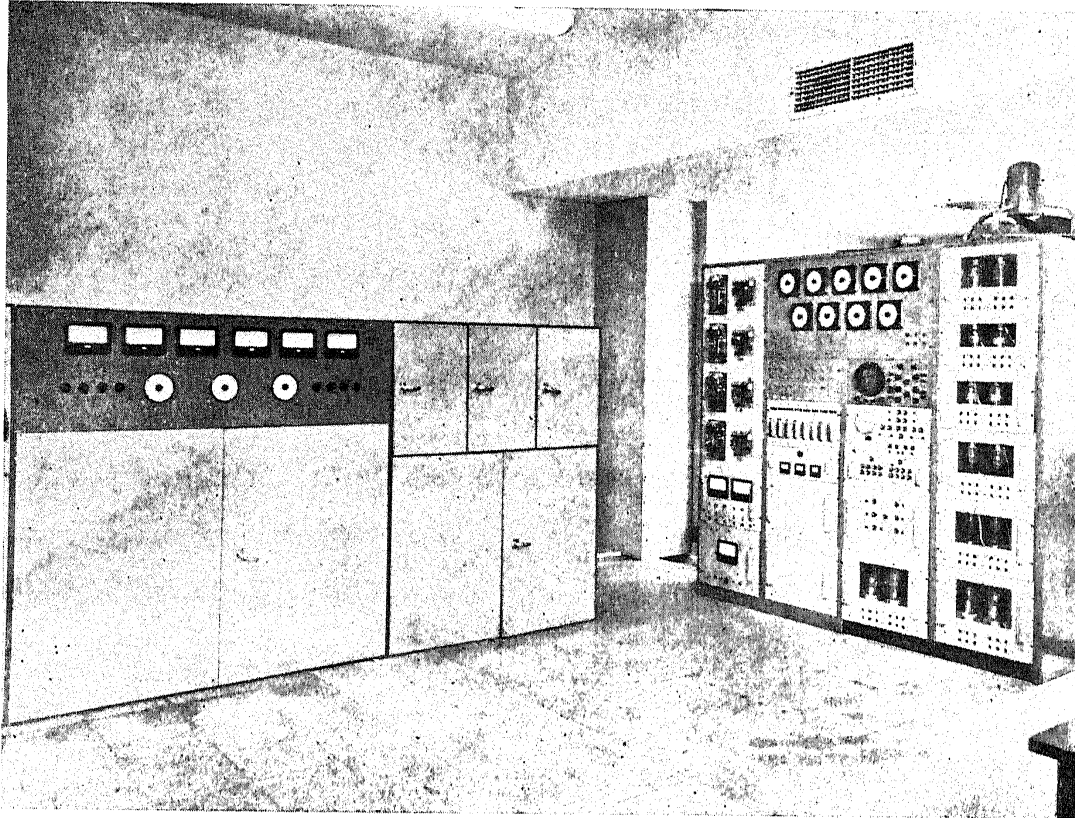FIG. 5. The Computer Assembly (with doors removed) showing some of the plug-in units.

FIG. 6.   The power supply units of the Computer.