SOUDAN 2 DATA ACQUISITION AND TRIGGER ELECTRONICS

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Abstract

The 1.1 kton Soudan 2 detector is read out by 16K anode wires and 32K cathode strips. Preamps from each wire or strip are bussed together in groups of 8 to reduce the number of ADC channels. The resulting 644 channels of ionization signal are flash-digitized every 150 ns and stored in RAM. The raw data hit patterns are continually compared with programmable delay patterns and adjacency conditions. The data acquisition process is managed in a system of 24 parallel crates each containing an Intel 8086 microprocessors, which supervises a pipe-lined data acquisition process. The 8086's also manage the local trigger conditions and can perform some parallel processing of the data. Due to the scale of the system and multiplicity of identical channels, semi-custom gate array chips are used for much of the logic, utilizing 2.5 micron CMOS technology.

Introduction

The Soudan 2 nucleon decay experiment is a multinational collaboration of Argonne National Laboratory, the University of Minnesota, Tufts University, Oxford University, and the Rutherford-Appleton Laboratory. The detector will be located in the Soudan iron mine in northern Minnesota. It will be 700 meters below the surface to reduce the cosmic ray background. The detector will have a total active mass of 1.2 ktons and will be surrounded on all six sides by proportional tube veto shield walls which will produce signals for through-going cosmic rays or cosmic ray interactions in the rock walls.

The main detector consists of 256 modules (1m x 1m = 2.56 high), each weighing 5 tons. Most of the mass of the detector comes from corrugated steel sheets (1.6 mm thick) which are stacked vertically to give a hexagonal close-packed array of holes. In each of these holes is a long resistive Hytrel plastic tube (16 mm diameter) which is insulated from the steel by mylar sheets. The tubes have electric potentials applied to them via narrow copper strips producing a graded electric field inside the tube going from -10 kV at the middle to grounded at the two ends. Each module is sealed and has high purity argon-CO$_2$ gas flowing through it. Ionization produced by particles traversing the tube drifts (with a velocity of 1 cm/sec) up to 50 cm down the tubes as a result of the graded electric field. Here the ionization is amplified at vertical anode wires, and the signal is read out from these wires and from horizontal cathode strips behind the wires. The detector will have a track resolution of 15 and 10 mm for anode and cathode readouts, respectively, and 2 mm for the dimension along the tubes.

Thus, the detector will have excellent topological tracking capabilities for low energy charged particles and electromagnetic showers expected from candidate nucleon decays and neutrino background events. In addition, the energy of particles observed is sufficiently low that they will stop inside the detector. The measurement of the ionization deposited as a function of track length allows the determination of track direction and yields information on the particle type.

Overview of Electronic Readout System

This section gives an overview of the electronic readout system to be used with Soudan 2. Figure 1 contains a block diagram of the major system components.

Fig. 1. Block schematic of Soudan 2 readout.

The end of the stack of hytrel tubes and steel sheets faces an orthogonal array of proportional wires and cathode busses, to provide X-Y information about the charge drifting down the tubes. The third orthogonal coordinate Z is obtained by a relative time measurement of the drifting charge. The proportional wire and cathode signals are amplified by thick film hybrid preamps, and preamp outputs (which appear as current sources) are bussed on twisted pair length 32 meters. Eight preamps are connected to each bus, in a scheme which avoids ambiguities. The events of interest are highly localized. This effectively multiplexes the readout of the detector and reduces the number of electronic channels by a factor of eight. The twisted pair summing busses drive conditioning-shaping amplifiers, and the outputs of these amplifiers are carried differentially on ribbon-twisted pair cable analog cards which perform digitization and storage.

The analog cards reside in 24 MULTIBUS data crates. Each analog card accepts 16 input signals. For each data channel there is an input buffer amplifier, a six-bit CHOS flash encoder (RCA 3300), and a CHOS static RAM (Hitachi 6116) of length 2048 locations. Thus, this system is capable of storing 300 usec of ionization history when clocked at 150 ns. Each analog card also has five CHOS gate

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arrays containing approximately 5500 gates of trigger
technology and the necessary gating logic tied to the
MULTIBUS backplane. Each data crate accepts 16 analog
cards giving a total of 256 digitization channels per

each data crate is managed by an 8086
microprocessor, which is implemented currently as an
86C50 card (Diversified Technology or Harris), a
single board microprocessor. The 8086 interacts with
the crate through the P1 bus on the MULTIBUS
backplane.

Each data crate has a compactor card which, in
addition to providing the data compaction, also
provides a CAMAC port to a CAMAC module which serves
the purpose of DMA's, interrupts, and program data
transfers to/from the host, a VAX 11/780 with a Jornay
-11 CAMAC serial branch highway interface. A 4K by
2-bit FIFO is used to buffer data transfer to/from the host through the CAMAC port. The anticipated
occupancy is less than 12 data stored in the RAM's on
an analog card. The compactor card contains a fast
(150 nsec clock) pipe-lined micro-sequencer which
serves each analog card with the operations: address,
data fetch, data compare to a preset threshold and place
overflow, DMA data and address into the FIFO.

Within each data crate there is a calibration
card which, under local processor control, can be used
to calibrate all the analog channels and verify the
trigger logic within the data crate. Each data crate
also has a trigger communication card to support
communication with the trigger processor crate. The
trigger communication card, in addition to sending
trigger requests to the trigger processor, provides a
1-bit data bus with a 4K FIFO for data transfer
to/from the trigger processor. The trigger
communication card also provides a slave programmable
interrupt controller (82C59) to facilitate inter-
processor communications and synchronization control
between a data crate and the trigger processor crate.

In the data crates, communication between analog
card, compactor card, calibration card, and trigger
communication card is accomplished by use of the P2
bus. The P1 bus is used only for communicating by the
processor, which offers several advantages; for
eiample, the data crates may have other cards which
interact only with the processor (floating point
processor, additional memory, disc controller,
etc.). Data acquisition, compaction, DMA to the host,
etc. all may proceed without interference with the
local processor, except to the extent "that the local
processor must be involved.

Analog Card

In this section, we present a more detailed
discussion of the analog card. It is implemented on a
six-layer MULTIBUS format PC board slightly oversized
in size. We have implemented it in CMOS to minimize
the power consumption.

With each of the 24 data crates, there are 16
analog cards, each of which accepts 16 channels of
data from the anode wire/cathode bus.

At the analog inputs, there are
differential buffer-amplifiers to reject common mode
noise from the ribbon twisted-pair cables. These
amplifiers nominally have a gain of 1; however, the
gain may be increased as high as 10 by external
jumers. The amplifier output drives a zero crossing
amplifier and also goes to a 6-bit CMOS flash encoder
which is clocked with 150 ns period, corresponding to
2 ns in the drift dimension. The flash encoder output
is written in CMOS static RAM every 150 ns. The RAM
space may be either 512 or 1024 addresses under
software control of the local processor. RAM address
is provided for data acquisition from P2, and the
flash encoder clock. is derived from the least
significant address bit.

The zero crossing amplifier in each channel
provides a logic level which is a logic 1 if there is a
pulse in the channel larger than the reference level
supplied to the zero crossing amplifier. These 16
signals serve as input to four custom designed CMOS
gate arrays (PDK-1000) each of which has approximately
1100 gates of logic devoted to timing and latching
live channels. Each PDK-1000 gate array has within it
the following:

1. Live channel register. A four-bit register, the
bits of which determine which channels shall be
live for trigger purposes. This register may be
used to gate off noisy channels and for trigger
logic verification purposes.

2. Trigger active time register. An eight-bit
register, the contents of which specify the
resolution time of trigger requests produced from this
card.

3. Active channel latch. A four-bit latch which,
after a trigger, contains latched information of
which channels are active, either before or after
trigger time by an amount of time called latch
active time.

4. Latch active time register. An eight-bit
register which contains the word defining the
latch active time.

5. The logic to performing the timing functions
relating to trigger and latch active timing.

All the registers and latches in the PDK-1000
gate array may be written/read from the local
processor. The PDK-1000 produces four outputs which
represent the active state of four live channels and
serve as four of the 16 inputs to the trigger logic
gate array PDK-2000.

The custom-designed PDK-2000 gate array provides
all the logic relating to generation of trigger
requests in response to patterns of active channels.
The PDK-2000 has an adjacency matrix which determines
the maximum number of live adjacent channels and
produces an encoded word representing that
adjacency. There are two multiplicity encoders, one
of which uses partial sums across card boundaries.
There are two multiplicity registers and an adjacency
register and comparators for multiplicity and
adjacency. The PDK-2000 gate array provides three
trigger requests, two of which represent multiplicity
and one adjacency, which are wire OR'd over the P2
backplane and transferred to the trigger processor
through the trigger communication card. The trigger
processor, when it sees a trigger request level raised
by a data crate, knows only that at least one of the
16 analog cards in that data crate has had its trigger
criterion satisfied by the pattern of input active
channels.

In addition to the trigger logic embodied in the
PDK-2000, there is an empty socket which has inputs
identical to those of the PDK-2000, but has four
trigger requests outputs to four wire OR-ed busses on
the P2 backplane. This extra socket may be used at a
later date for "afterthoughts" to provide trigger
requests for active channel patterns other than those
implemented in the PDK-2000.
Compactor Card

The compactor card is in reality 2 six-layer MULTIBUS cards, because the logic would not fit on one card. The compactor has an address register which provides addresses to the RAM's on the analog cards during data acquisition and compaction. In addition, there is a card pointer which is used during compaction to address an analog card. During compaction, the RAM address and data returned on the P2 data bus are latched for the data comparator at the same time that the next address is sent on the P2 address bus to the enabled analog card. The logic skips a cycle of the compactor clock when addresses corresponding to page boundaries are pointed to by the address bus to allow data to become valid. When the data rate is not in data acquisition or compaction modes, the CMOS memories on the analog cards may be memory mapped by the local processor and addressed through P1 bus for diagnostic routines. The compaction card has an interrupt register which interacts with the 8259 PIC on the 86065 card through 7 of the 8 interrupt lines on the P1 backplane, the eighth line being reserved for the slave PIC on the trigger communication card. A 16-bit crate status register is provided on the compact and readout card to allow 14 inputs, and operates on them logically to produce an output. This output is the logical variable which is the global trigger for the experiment. This signal is carried on a line on the trigger processor MULTIBUS P2 backplane to each data communication card in the trigger processor, and then over each trigger bus back to the trigger communication card in each data crate. Trigger is carried on the MULTIBUS P2 backplane to the compactor card where it begins the trigger countdown sequence prior to compaction. It is also necessary to interrupt the 8086 at the time trigger timeout is complete. There is a slave 8259 interrupt processor (PIC) on the trigger communication card to allow various other interrupts to be served, for such things as global abort, external interrupt, etc.

Operation

In this section, we describe the operation of the readout system and, in particular, the details of the 8086 microprocessor software. Trigger information is made available from the 24 data crates in parallel to a central trigger processor. A fast hardware trigger matrix decides on the basis of channel adjacency and multiplicity whether the event is of sufficient interest to store in the analog card RAM's and later compact and readout. The analog card digitization proceeds asynchronously in each of the 24 data crates in a manner that RAM's are a circular data buffer. When a trigger decision is positive, the digitization is continued for an additional 50 microseconds beyond trigger time. Thus a complete history from 50 microseconds before the trigger to 50 microseconds after the trigger is stored for each channel.

A program has been written for the 8086 microprocessor which services the readout and compaction of data from the analog cards. The program supervises the operation of the hardware compactor and synchronizes CAMAC I/O activity with the host. The program has been implemented as a set of interrupt service routines which handle conditions occurring in the compactor hardware. Host access to the FIFO buffer is controlled with the Compactor Gate Array Register (CSR). A special software protocol has been set up for exchange of variable length messages and data between the 8086 and the host via CAMAC.

The heart of the program is the trigger interrupt service routine. Upon receipt of a trigger, this routine first clears the FIFO buffer and then places some event identification at the top of the FIFO. It then address each of the 16 cards in the crate and reads a latch which indicates which channels on the card contain data. If a channel contains data, compaction is started on that channel and the program then halts pending receipt of one of two interrupt conditions, compaction done or FIFO full. If compaction is done, the next active channel is compacted. If the FIFO fills, the host must be notified to read out data before compaction can resume. The FIFO full interrupt service routine is called to set the CSR to allow the host access to the FIFO and then wait until the FIFO has been emptied before returning control to the trigger service routine. When compaction has completed on all cards in the crate, the host is again granted access to the FIFO buffer and the program polls the CSR to determine when the FIFO is empty. At this time, the trigger pending condition is cleared, and the logic is enabled to accept another trigger.

The 8086 architecture imposes the constraint that an interrupt service routine can itself only be
interrupted by an interrupt of equal or higher priority. Thus the following interrupt hierarchy was chosen:

1. FIFO full
2. Compaction done
3. Trigger
4. CAMAC 0
5. CAMAC 1

The use of the first three levels was discussed in the preceding paragraph. The CAMAC 0 and CAMAC 1 interrupts are used in the following way: A CAMAC 1 interrupt, generated by the host with an F30*AO CAMAC command, alerts the 8086 that the host wishes to send a message so that the microprocessor clears and enables the FIFO. The host then writes to the FIFO with an F13*AL CAMAC command. Meanwhile the 8086 waits for a CAMAC 0 interrupt which indicates end of data. This interrupt is generated by the host with an F13*AL. Upon receipt of this interrupt, the 8086 program will interpret the message and take the appropriate action.

A simple protocol has been defined to control exchange of data between the 8086 and the host. Each message consists of a variable number of 24-bit words. The first word in the message contains the message word count in the first 16 bits and the message ID in the next 8 bits. The remaining words contain the message. The message byte may be either positive or negative. A positive message number indicates data transfer from the 8086 to the host while a negative message number indicates data transfer from the host to the 8086. Five types of messages have been defined so far:

Message ID: 1 - Compressed data header
2 - Compressed data
-128 - COM/Analog register initialization
-124 - Variable reset
-120 - Program restart

The register initialization message is typically used to set the compactor threshold, set the trigger timeout and set trigger conditions on the analog cards. The variable reset message is used to assign a crate ID and the program restart message is used to transfer control to code which allows the 8086 program to recover from error conditions.

The host level data acquisition and control software is MIDAS, which interacts with the data crates via a serial CAMAC to UNIBUS interface. Data from a MULTIBUS data crate is transferred in DMA mode via 5-MHz byte serial CAMAC highway. Typical event sizes expected for Soudan 2 are 12 Kbytes and the anticipated data rate is of the order of 40 msec. The MIDAS system provides interactive event display, data monitoring, and storage for offline processing.

A complete set of diagnostic software has been written to provide hardware debugging tools for most of the major subsystems within the data acquisition electronics.

We have constructed a 3 data crate system for use in the quality control testing of the manufacture of the 5-ton Soudan 7 detector modules. This is currently operating with an external cosmic ray trigger system. We are currently constructing and testing the internal trigger for operation with the Soudan 2 detector.

References


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