Optimization of Single Halo p-MOSFET Implant Parameters for Improved Analog Performance and Reliability

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Abstract

The effect of Channel Hot Carrier (CHC) stress under typical analog operating conditions is studied for p-MOSFETs. Our detailed characterization results show that Single Halo devices not only show improved performance, but also are immune to CHC degradation under various operating conditions.

1. Introduction

Single halo (SH) MOSFETs are recently proposed for mixed signal applications in view of their superior analog performance such as gain, transconductance, output resistance etc [1]. In this work, we investigate the hot carrier degradation behaviour of SH and conventional p-MOSFETs using specific stress conditions appropriate for analog applications. The degradation of analog device parameters due to Cannel Hot carrier (CHC) stress and its implications on circuit operation are discussed.

2. Device fabrication

The devices used in this work are p-channel Conventional and Single Halo (SH) MOSFETs fabricated on the same wafer using bulk CMOS technology [2,3]. The channel implant (Arsenic) for conventional devices is carried out before the gate oxidation, while for the SH devices a channel implantation is done from source side after the gate stack formation. In our fabricated SH devices, Arsenic ions are implanted at different tilt angles (7°, 10°and 15°) with the dose and energy of the implant optimised to have identical V_t as that of conventional devices. Gate oxide (3.7 nm) was grown in dry O_2 ambient followed by *in-situ* anneal. Shallow SDE regions were formed using BF_2 implantation. The schematic of the fabricated SH device is shown in Fig. 1.

3. Experimental Set-up

A few of the recent studies [4] on hot-carrier effects for CMOS analog operation have tried to look at the circuit parameter degradation on the basis of single transistor stress experiments. MOS transistor in a typical analog circuit either operates as an independent current source or, an externally defined fixed current is forced through the transistor.

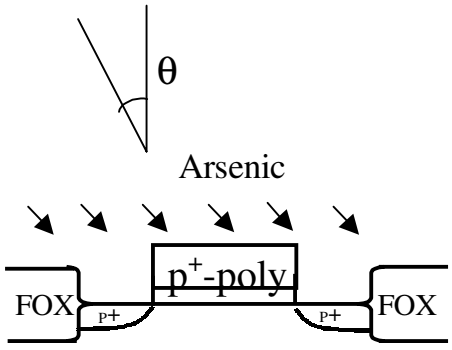

Figure 1. Schematic of single halo p-MOSFET structure

Unless otherwise stated, all the measurements done in this work are on isolated p-channel MOS transistors (SH and conventional) with SH devices fabricated with different tilt angle implantations (7°, 10°and 15°). The gate lengths are 0.35μm, width 10μm and the effective oxide thickness is 3.7nm.

For all the stress measurements, the applied drain voltage is 5.0V and the gate voltage applied is such that

the transistor is operating at $I_B=I_{B,max}$ condition, which is normally around $V_{GT}\approx$-1.1V.

AC small signal transconductance (g_m) is measured using HP4284 LCR meter at a frequency of 100KHz. After stress, g_m is measured for SH and conventional devices biased at identical V_{DS} and $V_{GT}(=V_G-V_T)$ as that of pre-stress values. For the charge pumping current measurements, the gate of the MOS transistor is connected to a pulse generator, with source and drain shorted. The drain current is measured with the substrate grounded. All the charge pumping measurements are done using variable base level measurements and at a frequency of 1MHz [5].

4. Results and discussion

A drain current shift $\Delta I_{D,sat}/I_{D,sat}$ obtained in a single device experiment appears as a current shift in an analog circuit [4]. The decrease in drain current under saturation conditions ($\Delta I_{D,sat}/I_{D,sat}$) with injected charge ($Q_{B,stress}=\int I_{B,stress}(t_{stress})dt_{stress}$), is shown in Fig. 2. The drain current is measured at V_D=-1V with V_{GT} fixed at 300mV for conventional devices. At identical stress V_{DS}, SH devices show substantially lower degradation compared to the conventional ones. The measurements are done at identical saturation drain current levels. It can be seen that 10° tilt angle devices show the least degradation.

The degradation effects in p-channel conventional MOSFETs is explained by Brox et. al. [6], assuming a stress induced trapping of electrons close to the drain. The length of the zone containing occupied electron traps, L_{damage} is a function of stress time t. The areal density of trapped charges is assumed constant within L_{damage}. Thus L_{damage} is directly proportional to the total trapped charge. The above assumptions hold even for the SH devices and a logarithmic time dependence in the degradation is observed, as shown in Fig. 3, for all the different tilt angles studied in this work.

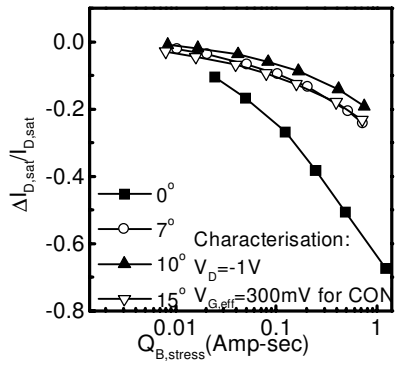

Figure 2. Dependence of drain current degradation on injected charge (Q_B).

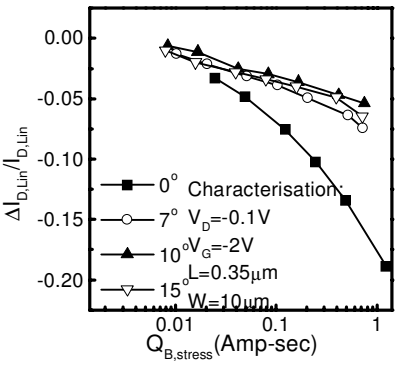

Figure 3. Degradation of drain current in linear region of operation with $Q_{B,stress}$.

The drain current degradation in the linear mode is directly proportional to the ratio of damaged region to the effective channel length, i.e. $(\Delta I_{D,lin}/I_{D,lin})\propto(L_{damage}/L_{eff})$ [7]. Thus the normalised drain current degradation in the linear region, i.e. the product of drain current degradation and effective channel length, is a direct measure of L_{damage}. As can be seen from Fig. 3, the $(\Delta I_{D,lin}/I_{D,lin})$ as a function of $Q_{B,stress}$ shows a logarithmic time dependence. The $I_{D,lin}$ is measured at V_D=-0.1V and V_G=-2V. The different slopes reveal that the ΔL_{damage} is consistently lower for all SH implant angles compared to the conventional devices, which is beneficial for analog operation.

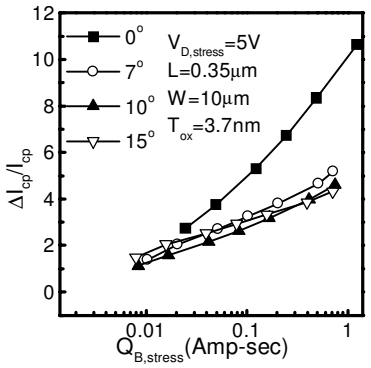

Figure 4. Charge pumping current as a function of injected charge, Q_B.

Charge pumping current is a sensitive monitor for the stress-induced interface states in the channel region. Fig. 4 shows the $Q_{B,stress}$ dependence of interface degradation (as monitored by charge pumping method) for different tilt angles. The observed trend is identical to the $\Delta I_{D,lin}/I_{D,lin}$, confirming that ΔL_{damage} is lower for the case of SH devices.

Another important parameter is the small signal AC transconductance (g_m) in the low gate voltage saturation regime. Fig. 5 shows the AC small signal

transconductance degradations as function of stress time for different tilt angle devices. The small signal g_m is measured at V_D=-1V, by applying a 10mV sinusoidal gate voltage, at a frequency of 100kHz. It was reported that the small signal transconductance is higher by about 20% for the SH devices compared to the conventional devices [1,8]. As shown in Fig. 5, the degradation in the small signal transconductance is also consistently lower for the SH MOSFETs. In Fig. 6, the stress time dependence of G_{DS}, for the same V_{DS} and initial I_{DS} values, for different SP and conventional devices is shown. It

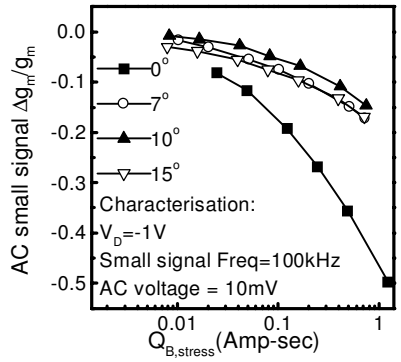

Figure 5. Time dependence of the AC small signal transconductance degradation measured in saturation.

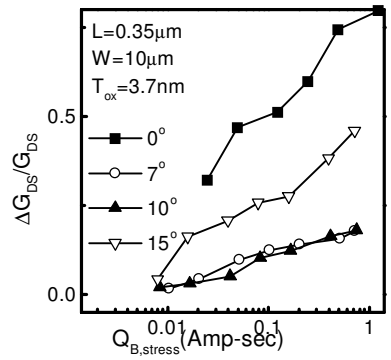

Figure 6. Drain conductance degradation of 0.35µm channel length devices with characterisation conditions as given in figure 3.

can be noted that the degradation is lower for SH devices, and that the degradation decreases with decreasing tilt angles. As shown, 15° tilt implant devices show a higher degradation compared to 7° and 10° cases.

Fig. 7 shows the percentage change in gain with injection charge. This parameter is a measure of the maximum achievable single device amplification. This result is consistent with Fig. 6 in the sense that the lower tilt angles are better in suppressing hot-carrier degradation for SH devices. The degradation effects of drain current as a function of drain voltage are shown in Fig. 8. SP devices show lower degradation compared to conventional devices with the least degradation occurring for implant angles of 7-10°. With increasing V_D, the degraded channel region contributes less to the overall saturation current degradation.

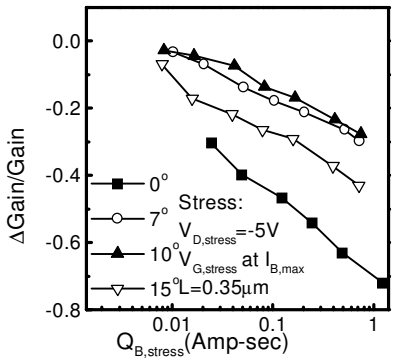

Figure 7. Small signal gain degradation of 0.35µm PMOS devices measured in saturation.

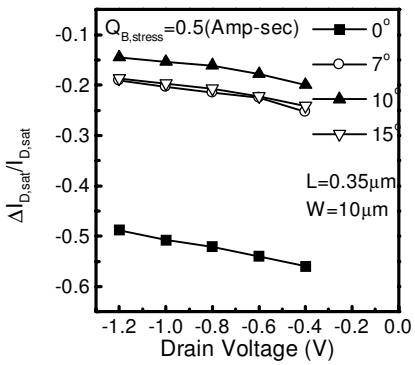

Figure 8. Operating point dependence of drain current degradation.

In Fig. 9, the stress induced offset voltage $V_{offset,hc}$ is plotted as a function of injected charge Q_B. $V_{offset,hc}$ is measured by changing the post-stress gate voltage to achieve pre-stress drain saturation current. Thus, a higher drain current degradation would lead to a larger change in the $\Delta V_{GS,eff,}$ which is detrimental to the analog CMOS operation. In the SH devices, as can be seen, the $\Delta V_{GS,eff}$ is lower under stress, indicating its suitability for analog applications.

Lateral electric field profiles for SH and conventional devices obtained from 2-D device simulations ISE-TCAD [9] are plotted in Fig. 10. The

SH devices show a more uniform lateral electric field profile along the channel, resulting in a lower peak electric field near the drain region, which can be attributed to the observed suppression of CHC degradation in SH devices.

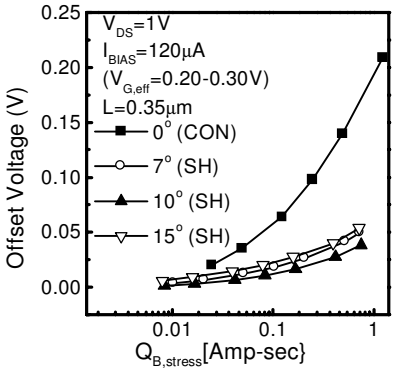

Figure 9. Measured values of the stress-induced offset voltage $V_{offset,hc}$ vs. Q_B of a 0.35μm devices at different tilt angle values.

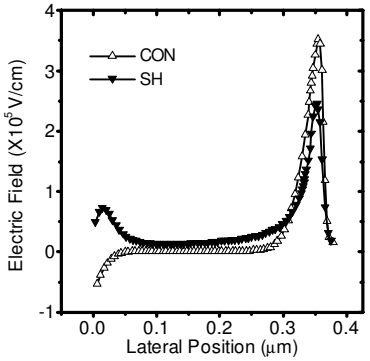

Figure 10. Simulated lateral electric field along the channel for conventional and SH (10°) devices. Channel length is 0.35μm.

5. Conclusions

The Channel Hot Carrier (CHC) induced device degradation has been measured under typical analog operating conditions for deep sub-micron p-MOSFETs. Different device degradation parameters have been compared, for different analog operation cases. The SH devices show suppression of various analog device parameter degradation compared to conventional devices, under identical stress conditions. In the SH devices the lower tilt angle (7° and 10°) cases show less degradation compared to higher tilt angle implantations (15° tilt), studied in this work. This work clearly shows that SH devices therefore are best suited for analog applications.

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