Optimization of Sub 100 nm Γ-Gate Si-MOSFETs for RF Applications

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This paper presents characterization and simulation studies on the RF performance of the Γ (Gamma) gate MOSFETs. The Γ-gate MOSFET offers the advantage of reduced gate resistance, a critical parameter in high frequency circuits. The aim of this study is to identify the optimum Γ–gate extension length from the gate and drain resistance point of view in aggressively scaled CMOS.

NEED FOR CMOS IN RF APPLICATIONS

By the end of the 20th century we have seen an explosion in the application of "wireless" devices. With the increasing popularity of wireless communication systems like cordless phones, wireless modems, and personal communication networks, higher levels of RF component integrations are required to reduce size and cost of products. While CMOS has been the dominating technology for the base band chipsets, the latest evolution in CMOS technology, with shorter channels and faster devices, has made MOSFET a viable choice for RF application, especially for the frequency in the low GHz region [2]. CMOS technology is attractive because of the low cost, high integration and easy access to the technology. However, gate resistance in aggressively scaled CMOS technologies must be taken into account and modeled correctly for accurate benchmarking of the CMOS technologies for RF applications [3]-[5]. For optimized RF performance, the gate resistance has to be low, even when the gate areas are small. R_g consists of two parts, the distributed gate electrode resistance (R_{geltd}) and the distributed channel resistance as seen from the gate (R_{gch}), as shown in the Fig. 1 [4].

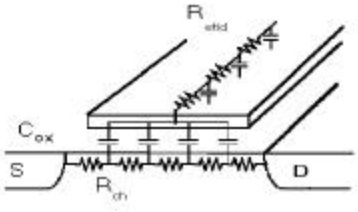

Fig 1: The gate resistance model used in RF modeling

$$R_g = R_{geltd} + R_{gch} \quad (1)$$

Now, as the MOSFET gate dimensions are reduced, the effective gate resistance increases. Larger gate resistance can substantially degrade the RF high-speed performance. The two figures of merit used for high speed circuits are the f_t and the f_{max}. These represent the frequencies at which current and the power gain, respectively, are extrapolated to fall to unity. For the MOSFET these are defined as follows:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (2)$$

Where C_{gs}, C_{gd} and g_m are the gate to the source capacitance, gate to drain capacitance and the transconductance respectively. The power unit gain frequency f_{max} can be roughly expressed as

$$f_{max} \approx \frac{1}{2}\left(f_t \Big/ 2\pi r_g C_{gd} \right)^{\frac{1}{2}} \quad (3)$$

Where r_g is the gate resistance. To reduce the gate resistance, currently, various silicides are being investigated. The problem with this technique is that, as the line width is reduced below 100nm, due to lack of nucleation sites in the C-49 to C-54 structure of silicides, the sheet resistance increases [6]. Even with Co silicides, which are found to be independent of the line width even below 100nm, the problem of increased gate resistance, due to smaller dimensions still persists [7]. This paper summarizes our studies on the RF performance of the Γ-gate MOSFET.

The process simulation was done in TSuprem4 and the device simulations were done in MEDICI, after which the

simulated device's electrical characteristics were matched with the actual results. For various stack lengths, the important RF parameters such as scattering (s-) parameters, forward current gain (H_{21}), the unilateral transducer gain $G_{tu_{max}}$, f_t and f_{max} were extracted. From the frequency response of different Γ-gate MOSFETs, the best-suited extension length for the Γ-gate MOSFET is predicted.

FABRICATION

After LOCOS, 230nm poly-Si was deposited on top of 25nm (PSG) and 1.5nm of SiO_2. The V_{th} adjust implant was performed by Indium and Boron. A gate oxide of 2.7nm thickness was then grown. The poly-Si spacer was then formed by the deposition of 58nm undoped poly-Si, followed by RIE etch-back. A LATI was then done with Phosphorous, at 70^o to shorten the drain extension length. The source extension was doped with Antimony. After the LTO spacer formation, S/D and poly-Si gate implant was performed. The final samples were annealed at 950^{o}C for 15 to 20s. The spacer gate and the dummy stack are connected by a standard two step Ti silicide process as shown Fig 1. For further details of gamma gate MOSFET fabrication, please see K.H.To et al., [1].

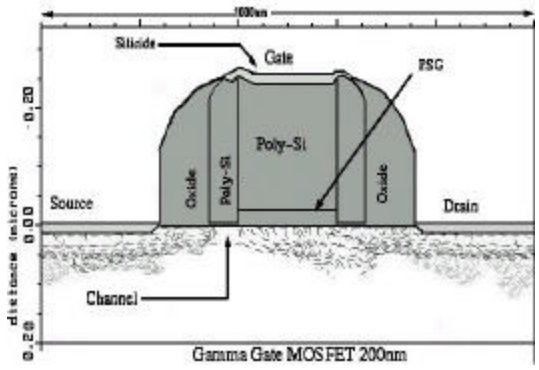

Fig 2: Structure of the 60 nm channel length Gamma Gate with 200nm stack length.

CHARACTERIZATION AND SIMULATIONS

The structure was simulated in the process simulator *TSUPREM4*. The *I-V* characteristics of the device, both experimental and simulated are shown in Figs. 3 and 4. Considering the novel fabrication process involving the solid-phase diffusion, and the 60 nm gate length, one can see a reasonable match between the simulated and the experimental results. The simulated device had a V_{th} of 0.53V while the fabricated device had a V_{th} of 0.51V.

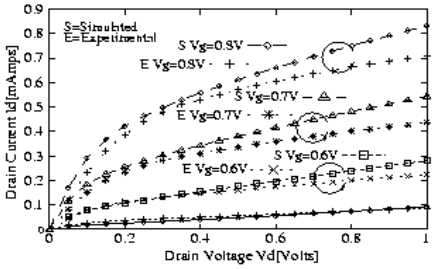

Fig 3: I_d-V_d for 200nm stack length simulated and experimental characteristics for 60nm channel.

The experimental I_{on} at V_d=1.0V and the simulated value of I_{on} at the same voltage were found to be 0.23mA/μm and 0.28mA/μm respectively at V_g=0.5V. We simulated devices with various dummy stack lengths and for each stack length the electrical parameters were extracted in the *MEDICI* device simulator.

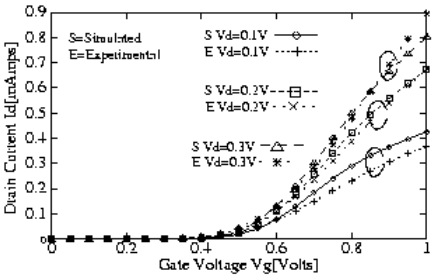

Fig 4: I_d-V_g for 200nm stack length simulated and experimental characteristics for 60nm channel.

RESULTS AND DISCISSION

The s-parameters of the Γ-gate n MOSFET can be found by defining the input and output port as the gate and the drain respectively [8][9]. The device is biased at a V_g of 1Volt and a V_d of 1 Volt and an ac-signal of 0.1 Volts with varying frequency is applied to the gate of the n MOSFET.

To evaluate the device performance at high frequency, two criterions were used: the forward current gain $|H_{21}|$ and the unilateral transducer gain $G_{tu_{max}}$.

$$H_{21} = \frac{-s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}s_{21}} \quad (4)$$

$$G_{tu_{\max}} = \frac{|s_{21}|^2}{(1-|s_{11}|^2)(1-|s_{22}|^2)} \quad (5)$$

The results of simulations are included in Figs. 5 and 6. With the extracted s-parameters, f_t, the cutoff frequency was calculated and plotted. The $|H_{21}|$ method extracts f_t by plotting the $|H_{21}|$ *vs. f* in the log scale, the resulting plot is then curve fit by linear regression. The slope *m* and the intercept *c* of this fit are used to calculate f_t using

$$f_t = 10^{-c/m} \quad (6)$$

The H_{21} method assumes that the roll-off of the $|H_{21}|$ in the $|H_{21}|$ vs. f plot is –20dB [2].

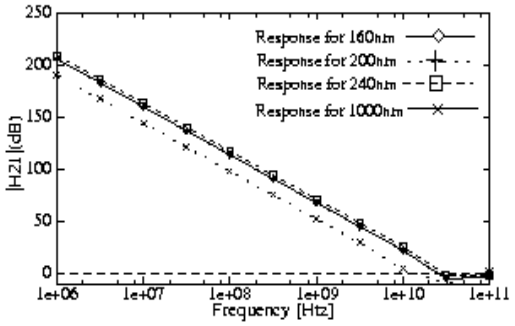

Fig 5: $|H_{21}|$ vs. frequency for various stack Γ- gate lengths.

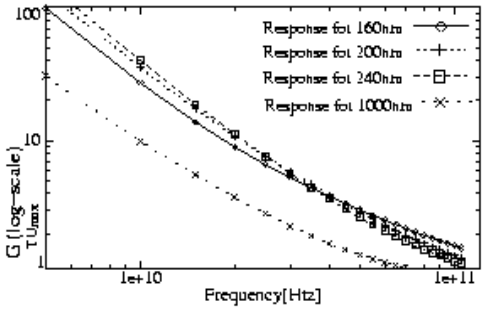

Fig 6: $G_{tu_{\max}}$ vs. frequency for various Γ- gate stack lengths.

As can be clearly seen in Figs. 5 and 6, the RF performance of the n-MOSFET degrades with an increase in the stack length, since f_t falls from 2.53×10^{10} Hz, for the 200nm stack to 1.38×10^{10} Hz, for the 1000nm stack. Also, from the figures it is evident that the 240nm-stack length has a higher f_t at 2.80×10^{10} Hz. The plot of $G_{tu_{\max}}$ *vs.* f also shows a similar trend. It can therefore be concluded that the Γ-gate MOSFET would have the best performance for stack lengths of around 240nm, where the drain resistance is still under control.

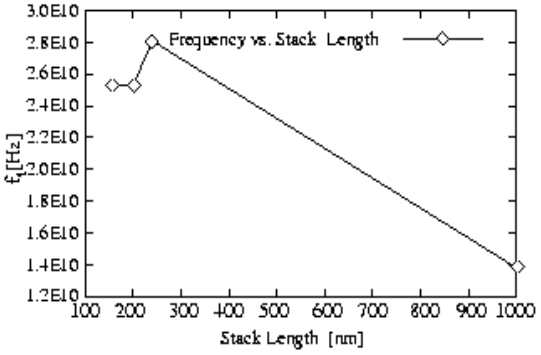

Fig 7: f_t vs. frequency for various Γ- gate stack lengths

It can be seen from Fig.7 that, as the drain extension of the Γ gate increases in length, the RF performance of the n-MOSFET degrades. This implies that for Γ-gate n-MOSFETs, smaller stack lengths would certainly perform better than longer stack lengths in the high frequency regime. Yet this does not mean that the reduction in the gate resistance has no effect on the MOSFET, in fact as the small signal model of the MOSFET suggests, the gate resistance would certainly affect the f_t. A better measure of the efficacy of the Γ-gate MOSFET would be its comparison with a standard 60nm MOSFET with the gate length of 60nm, which would bring out the effect of the increased gate resistance.

For the simulated device, the value of $G_{tu_{\max}}$ was calculated using s parameters from Eq.5. The result of the simulations is given in Fig 6. The plot of $G_{tu_{\max}}$ *vs. f* again shows the trend predicted before: for longer stack length the RF performance of the Γ-gate MOSFET is degraded and the value of f_{max} falls from a figure above 100GHz to 70GHz.

STABILITY OF DEVICE

While the variations in s-parameters cannot give a clear picture of whether performance varies with the stack length, the stability of the MOSFET is definitely affected. The stability factor K and the s-matrix Δ were calculated from the s-parameters with Eq.7 and 8 and checked against the conditions listed in Eq.9 to determine stability for an amplifier.

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} \quad (7)$$

$$\Delta = s_{11}s_{22} - s_{12}s_{21} \quad (8)$$

$$\left.\begin{array}{l} K > 1 \\ \Delta < 1 \end{array}\right\} \text{ Conditions for Stability} \quad (9)$$

K and |Δ| for devices of different stack length, at various frequency are plotted in Fig. 8, and in Fig. 9 respectively. The |Δ| vs. f curves were below |Δ|=1 line for all the stack lengths and they decreased monotonically with increasing frequencies. However, the K vs. f curves increased monotonically, and actually shifted to the left with increasing stack length. This shift implies that devices with long stack lengths meet the conditions of stability at a lower frequency than their short stack length counterparts.

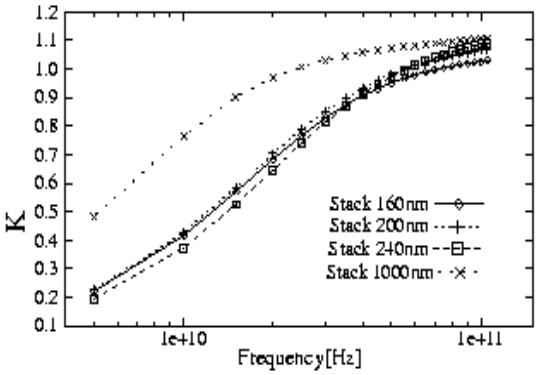

Fig 8: K (stability factor) vs. frequency for various Γ- gate lengths.

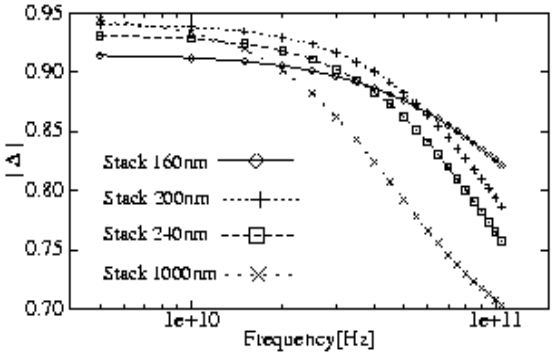

Fig 9: |Δ| vs. frequency for various Γ- gate lengths.

CONCLUSION

The Γ-gate n-MOSFET offers the advantage of reduced gate resistance due to the large gate area, while the scaled conventional MOSFET performance is degraded due to a reduction in gate dimensions, with the resulting higher gate resistance. The optimal stack length for the gamma gate MOSFET has been identified in this work from simulations. It has been found that though the devices with longer stack reach stability at a lower frequency yet stack length of the order of 240nm and less would be ideal for GHz range when factors like forward current gain and unilateral current gain are taken in to consideration.

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