A MODIFIED GATING LOGIC TO IMPROVE THE SPEED OF OPERATION OF DOUBLE RANK COUNTERS

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Abstract

The speed of operation of double rank counters can be increased by a suitable modification of the gating logic now being used. The improvement in speed, predicted on theoretical grounds, has been experimentally verified. The prescribed logic enables the use of both the ranks of the counter to advantage, one rank counting in the normal, and the other in the reverse fashion.

Introduction

The use of counters, in digital computers, for iterating a sequence of micro-operations a specified number of times is well established. A design requirement for such a counter may be prescribed as follows: Let t be the total time taken by the counting pulse to set up all the digit stages of the counter. Then t must be less than the time taken for one complete iteration of the sequence. Clearly, the faster the computer and smaller the length of the sequence being iterated, the smaller is the permissible value of t. In this paper a gating logic is described to reduce t much below the value required by double rank counters now being used.

In the counters normally being used, a situation may arise during the process of counting when the counting pulse can give rise to a carry chain from the lower to the higher order digit stages. This cumulative action of the carry will cause a delay in the setting up of the higher order digit stages of the counter. One way of reducing this time delay (*i.e.*, setting up time t) is to let the carry propagation be determined by the set up of the digit stages prior to the arrival of the counting pulse. The carry can thus be channelled through external circuits. With a single rank counter,[1] however, such an arrangement, requiring accurate timing of pulses, complicates the design. It was, therefore, considered worthwhile to investigate the possibility of working out a similar system with double rank counters.

The double rank counter.—The design philosophy of double rank counters originated with the computer group of the Institute of Advanced Studies[2]

(I.A.S.) at Princeton. Since then this type of counter has been used in almost all the computers of the I.A.S. type. An attractive feature of such a system is that one can ensure reliability by completely avoiding transient storage and gating elements.

In double rank counters two flip-flops are necessary for each digit stage. Counting is done by the mutual exchange of information between the corresponding flip-flops of the two ranks and requires a cycle of two pulses for each count. One rank, the false rank,* serves as a buffer or temporary storage space while the actual count is obtained in the true rank. Rules are formulated stating the conditions for gating from either rank to the other. A detailed analysis of the prevalent systems of gating arrangement has been published by Ware[3] and by Brown.[4] The cumulative carry delay is, however, not avoided in any of the systems described by them.

A gating logic for avoiding carry delay.—Consider a single stage counter containing a true (T) and a false (F) flip-flop. Counting is done by gating the number from the true to the false (down pulse) and the false to the true (up pulse). Since the true flip-flop has to change for every up pulse it is evident that one of the two, $T \rightarrow F$ or $F \rightarrow T$ transfers should be in the complement form† while the other is direct. For definiteness, let us assume that the gating from the true to the false flip-flop is direct and from the false to the true is in complement form. This can be symbolically represented as,

$$T \overset{d}{\rightarrow} F$$

$$F \overset{c}{\rightarrow} T$$

For a multi-stage counter the conditions for gating $T_i \rightarrow F_i$ and $F_i \rightarrow T_i$ can be readily derived in the following way. If one has to avoid the carry delay completely when the gating from the false to the true takes place, it is evident that this gating has to be done in parallel. We can, therefore, write down the condition of gating from the false to the true rank as,

$$F_i \overset{c}{\rightarrow} T_i, \text{ for } i = 0, 1, \ldots, n \text{ with every up pulse.} \qquad (1)$$

The above condition simply implies that the counting has actually been accomplished by the down pulse preceding the up pulse. Now the T_i of a particular stage i will change its state during any count if in the previous

* The terminology, true rank and false rank is taken from Ware. See reference 3.

† In this paper complement always means 1's complement.

setting of the true rank, the flip-flops from T_{i-1} down to T_0 have all been 1's. But T_i can change if and only if F_i changes. The rule for $T_i \rightarrow F_i$ can now be readily formulated as follows:

$$T_i \overset{d}{\rightarrow} F_i \text{ by the down pulse if all the stages } T_{i-1} \text{ to } T_0 \text{ are 1's.} \qquad (2)$$

Combining (1) and (2), we have the complete gating rules as,

$$\text{(i) up pulse } F_i \overset{c}{\rightarrow} T_i, \text{ for } i = 0, 1, \ldots\ldots, n$$

$$\text{(ii) down pulse } T_i \overset{d}{\rightarrow} F_i, \text{ for } i = 1, \ldots, n, \text{ if the digit stages } T_{i-1} \text{ to } T_0 \text{ are all 1's} \qquad (3)$$

$$\text{down pulse } T_0 \overset{d}{\rightarrow} F_0.$$

A logical diagram satisfying these gating rules is shown in Fig. 1.

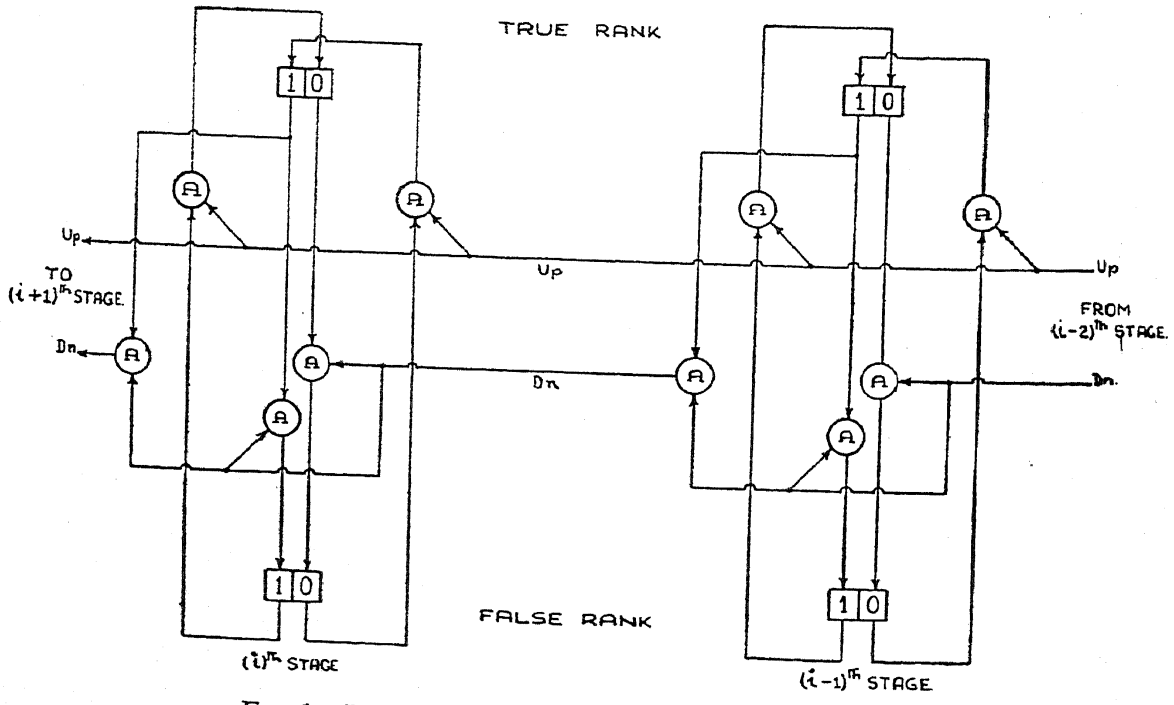

FIG. 1. Logical Diagram of Double Rank Counter.

Some distinct advantages of this system of gating can be easily seen. First of all, no carry delay is involved in gating from the false to the true rank by the up pulse which may be termed the counting pulse. Even in the gating from the true to the false rank, there is very little carry delay involved, as the carry is channelled through external circuits. If cathode follower type of negative 'And' gates are used, the carry delay time will be negligible

for a six-stage shift counter of a typical digital computer. Secondly, since the false rank always contains the complement of the number in the true rank, the false rank counts down from the final number while the true rank counts up to it. Thus a single counter can serve the purpose of additive and subtractive counting at the same time.

In Table I, columns 2 and 3 give the readings of the true rank and the false rank of a four-stage counter just after the down shift has taken place. Column 4 also shows the number in the false rank when the gating arrangement is reversed, *i.e.*,

$$\text{(i) up pulse } F_i \xrightarrow{d} T_i, \text{ for } i = 0, 1, \ldots, n$$

$$\text{(ii) down pulse } T_i \xrightarrow{c} F_i, \text{ for } i = 1, \ldots, n \text{ when } T_{i-1} \text{ to } T_0 \text{ are all 1's.}$$

$$\text{down pulse } T_0 \xrightarrow{c} F_0. \tag{4}$$

TABLE I

Countings of the true and the false ranks of a four stage counter

Decimal equivalent of the number in the true rank	Number in the true rank	Number in the false rank	
		$F \xrightarrow{c} T, T \xrightarrow{d} F$	$F \xrightarrow{d} T, T \xrightarrow{c} F$
0	0000	1110	0001
1	0001	1101	0010
2	0010	1100	0011
3	0011	1011	0100
4	0100	1010	0101
5	0101	1001	0110
6	0110	1000	0111
7	0111	0111	1000
8	1000	0110	1001
9	1001	0101	1010
10	1010	0100	1011
11	1011	0011	1100
12	1100	0010	1101
13	1101	0001	1110
14	1110	0000	1111
15	1111	1111	0000

This table makes it quite clear that counting actually takes place in the down shift from the true to the false rank. If the count in the false rank is

of no consequence, one can decide arbitrarily for each digit stage, which of the two transfers F → T or T → F is to be in complement form. In this case, however, it is to be expected that the numbers in the false rank will not follow the usual sequence.

EXPERIMENTAL RESULTS

To verify experimentally the advantage of the gating logic described, a four-stage counter was built and its performance was compared with that of a prevalent type of such counter. The initial condition was set up so that a single counting pulse gave rise to a carry chain from the lowest to the highest order stage of the counter. The setting up time was then measured with respect to the counting pulse. In the logic described in this paper, there can be a setting up delay only in the down shift, as in the up shift information from all the digit stages is gated in parallel. Therefore, measurement was made only when the number was being gated from the true to the false rank of the counter. It was found that the total setting up time in the new design was virtually the same as the setting up time of a single flip-flop, whereas, with the old design the time delay was nearly equal to four times this.

Counting from a predetermined number.—In some applications it is necessary for a counter to have arrangements so that counting may start from a predetermined number. For either of the gating arrangement 3 or 4 this can be accomplished by simply gating the predetermined number *plus* one in the false rank of the counter in complement (gating arrangement 3) or in true form (gating arrangement 4) and start the counting cycle with the up pulse. This is, of course, the same thing as gating the number without adding one in the false rank and applying one cycle of up and down pulse externally. However, if the carry delay consideration is not too stringent, the adding of one or the external cycling can be avoided by interchanging the role of the true and the false rank flip-flops, described before, in the following manner:

$$\text{(i) down pulse } T_i \overset{c}{\rightarrow} F_i \text{ for } i = 0, \ldots, n, \text{ in parallel.}$$

$$\text{(ii) up pulse } F_i \overset{d}{\rightarrow} T_i \text{ for } i = 1, \ldots, n, \text{ if all the stages } F_{i-1} \text{ to F are zeros.}$$

$$\text{up pulse } F_0 \overset{d}{\rightarrow} T_0. \qquad (5)$$

In this case counting is accomplished by the up shift instead of the down shift as in the other cases. For counting from a predetermined value

the required number is to be gated in the true rank of the counter and the counting cycle can be started with the down pulse first.

Conclusion

The gating logic for double rank counters was developed in an attempt to design a shift counter suitable for operation with a fast digital computer. Several other possible uses of such a counter have also been indicated in the paper. It has been found that the proposed change in the gating logic does not increase the complexity of the design of double rank counters any more than what is needed with the prevalent gating arrangement.

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