A FAST CIRCUIT MODULE FOR DIGITAL SYSTEMS

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Abstract

This paper describes an AND-OR-INVERT module developed for the OLDAP computer designed and being built at the Tata Institute of Fundamental Research. To obtain the maximum speed out of available transistors, the circuit makes use of antisaturation and anti-cut-off techniques. The effect of different components on the transient response of the circuit is described. Detailed results of DC tolerance analysis and noise margins are included. The module which uses only indigenous components should be useful in any general digital system where speed is an important requirement.

1. Introduction

Reasons for the general practice of using in digital computers only a few types of basic modules or building blocks which are interconnected to form more complex units are well known and are valid for any large electronic system that permits this approach. For digital systems in general, a basic logical unit (such as an AND-OR-INVERT complex) is standardised, such that flip-flops, selectors, counters and other logical units can be realised out of these modules. The only exceptions are special circuits such as current and voltage drivers.

Optimisation of design, with attention to economy, speed, noise sensitivity, logical power, physical size and power dissipation of the module reflects directly on the overall performance, reliability and cost of the system.

Two important requirements for such a module are that it should be permissible to: (*a*) cascade these modules with strings of indefinite length and (*b*) "fanout" from (the output of) any one element into (the inputs of) a number of others.

The basic circuit module should thus incorporate at least one stage of transistor amplification (and DC level restoration if necessary) automatically providing logical "inversion". For logical completeness, Boolean "AND" or "OR" capability must also be provided. Resisters, diodes, transistors or a combination of these can be used to perform these logical operations. This paper describes the basic logic circuit which constitutes the major hardware of the OLDAP computer. The OLDAP computer is an On Line Data Processor which is a special purpose transistorised digital computer presently under design at the T.I.F.R. It is primarily intended as a real time control computer and will also be able to function as a satellite to a much larger central processor.

Of the several types of circuits possible, a Diode Transistor-Logic module was chosen as the most suitable.[1]

The design objective was to use only indigenous components, and to attain increased speed of operation even at the cost of circuit complexity, within reasonable limits. Antisaturation and anti-cut-off feed back techniques are therefore used. It may be noted that these involve only a marginal increase in the overall cost of a module.

2. General Design Considerations

An AND-OR-INVERT configuration which provides two-level logic was chosen as opposed to single-level Nand or Nor configurations. The number of transistors is the same for both single-level and two-level logic, and the additional versatility of two-level logic more than offsets the cost of the few additional diodes and resistors that it entails.

Operation in the saturated mode with presently available transistors would have resulted in abnormally low speeds. Prevention of saturation eliminates the major limitation to speed imposed by minority carrier storage in the base region.[2] One major objection to operation in the non-saturated mode is the reduction in noise margins. However, even this is qualified by the fact that most of the experimental noise models, which form the basis for the above conclusion, are not fully valid in an actual system. Other factors concerning power dissipation, output impedance and circuit complexity are comparatively less significant.

Turn-on delays are eliminated by preventing the transistor from getting cut off, even in the "off" state. A feedback base drive ensures that the transistor draws a low current in this state, and has the additional advantage of a regulatory effect on the output voltage level.

It would be desirable to attain the highest permissible fan-in and fan-out capability for the module, consistant with fast and reliable operation. While high fan-ins and fan-outs tend to reduce module speed due to capacitive loading, they might result in higher system speeds, due to the smaller number of stages required for any function. In general, a more or less arbitrary compromise has to be effected, the upper limit bring set by D.C. considerations.

There are several different ways in which noise margin has been defined. Roughly, noise margin in a digital circuit is the amount of noise that can be present at the input, without causing output malfunctions.[3] Because of the variety of ways noise can arise (inductive and capacitive pick-up, resistive leak-through, ground noise, etc.)[4-7] and the difficulty of estimating or simulating the noise expected in an actual system, there is no generally agreed method for specifying the noise margins for a circuit. A rough D.C. measure will be the minimum worst case margin between the expected output voltage of the driving circuit and the input required by the driven circuit.

The deterioration in stage delay caused by excessively high noise margins, due to the finite rise and fall of the input and output wave forms is another important factor to be considered.

3. CIRCUIT OPERATION

Figure 1 shows a circuit diagram of the inverter. Diodes d_1 perform the AND function while diodes d_2 constitute the OR gates. d_3, d_4 and d_5 are the level shifting diodes. R_4 provides the turn-off current drain. Diode d_6 is the antisaturation clamp diode, while d_7 supplies the feedback current for maintaining a steady collector current in the transistor in the "Off" state.

Turn-On.—During the "off" state, circuit conditions are as follows: At least one diode d_1 is forward biased in each AND gate, its forward current being supplied by the preceding stage. All diodes d_2 are reverse biased. The current through d_3 is the sum of the currents supplied through d_7 and R_2. Part of this current flows through R_4, the remaining being sufficient to keep T_1 in a state of low conduction, due to the feedback current through d_7.

Application of appropriate positive voltage step at the inputs causes all diodes d_1 in at least one AND gate to cut off, after the stored charge is drained away. This causes atleast one diode d_2 to turn on, supplying additional base current to T_1 which now conducts heavily. The collector voltage falls only until d_6 is forward biased, preventing saturation. Diode d_7 gets

reverse biased even earlier. The collector current is the sum of the load current, and the currents flowing through R_5 and d_6.

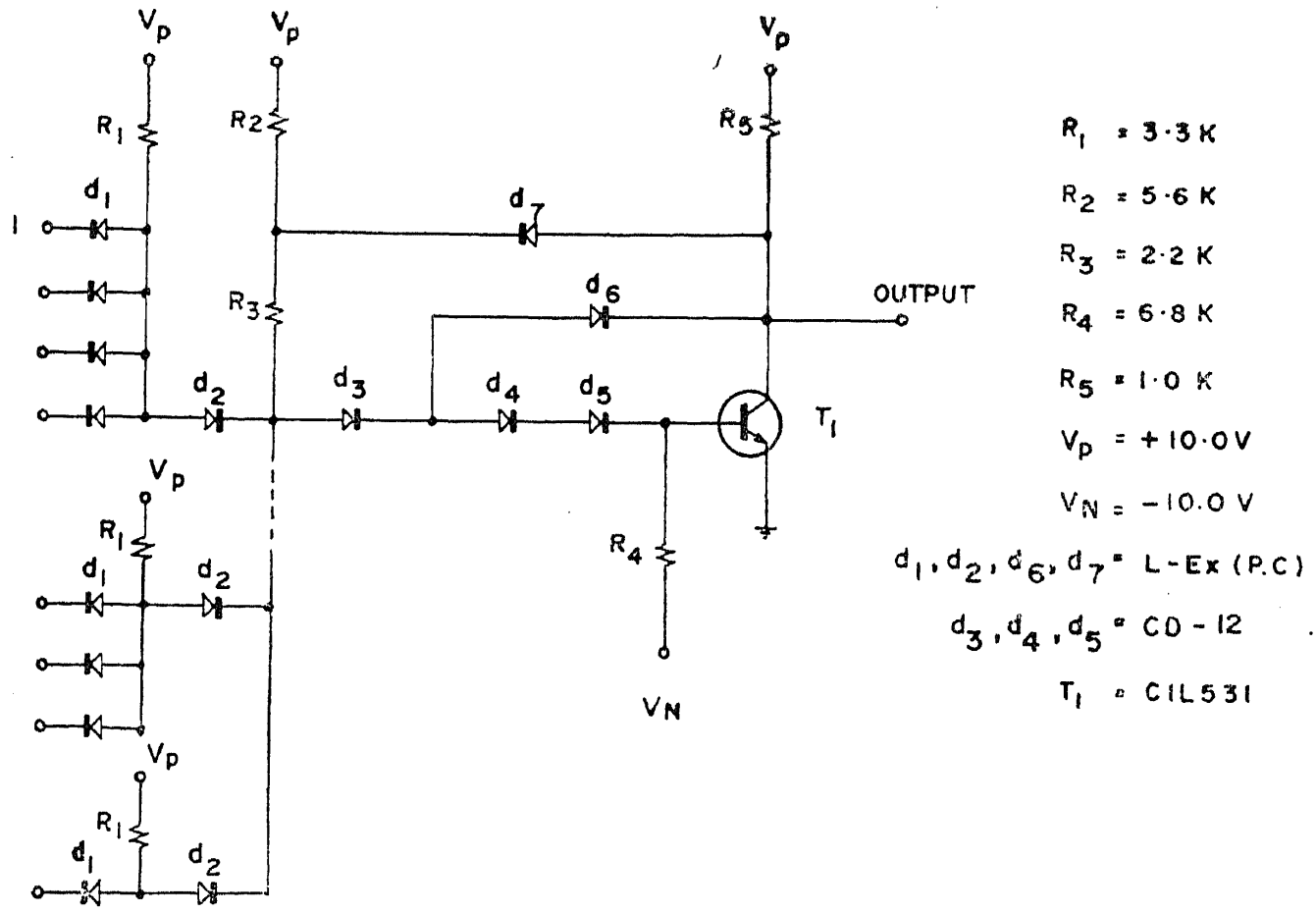

FIG. 1. The Basic logic module.

Turn-Off.—A negative voltage step at input 1 causes d_1 to conduct, turning d_2 off. Since the current supplied through R_2 and R_3 is less than the current through R_4, the difference is drawn as turn-off current of T_1, draining off its base charge. Stored charge of d_6 is swept off along the path $R_5 - d_6 - d_4 - d_5 - R_4$. The collector voltage then rises till d_7 is forward biased, after which it stabilises due to feedback. There is a small overshoot due to the delay in the feedback loop.

Transient behaviour.—For purposes of analysing the transient behaviour, this circuit may be visualised as consisting of two parts: the diode logic network and the level restoring inverter. Quantitative transient analysis of diode gates has been done.[8] Its most important implication is the effect of charge storage in switching diodes. Briefly, in an OR or an AND gate, the output state should be independent of the number of conducting diodes, changing only when all of them cutoff. If the fan-in is n, a transition from a state where all n diodes are conducting, to one where $(n - 1)$ diodes are cutoff, should not be noticeable at the output. In actual practice, however, the stored charge in these $(n - 1)$ diodes flows through the output circuit (input of the inverter) and the conducting diode, the current ratios being

determined by the relative impedances of these paths. In case this charge is sufficient to alter the state of the inverter transistor, a spurious response will result at the final output, its duration being equal to or less than the reverse recovery time of the switching diodes. Evidently, this can give rise to serious circuit malfunctions, particularly in the OR-stage where the impedence levels are higher. The inequality to be satisfied for avoiding such malfunction is

$$(n-1)\,Q_d < Q_t$$

where Q_d and Q_t are the stored changes in the diode and transistor respectively, in the on-state.

Another indirect effect of this phenomenon is the materialization of a low impedance path between the switching input and the steady state input through the switching input diode and the forward-biased diodes. Consequently, switching of the module connected to this input slows down very appreciably.[9] The choice of a fast recovery diode for switching eliminates this problem.

The function of the level shifting diodes (d_3, d_4 and d_5) in the base circuit of the inverter is quite different. One might alternatively use a resistor for level shifting, but the highly non-linear nature of the effective base-emitter capacitance and its high value during switching slow down the circuit very appreciably. Use of a speed up capacitor, while being to some extent helpful, introduces all the attendant problems of using a capacitor in a DC circuit. Use of diodes with appreciable reverse recovery times is an ideal solution.

The antisaturation clamp diode d_6 speeds up circuit operation by getting forward biased and preventing the collector-base junction from being forward biased. It is thus pointless to use this technique unless the reverse recovery time of this diode is appreciably less than the storage time of the transistor. Similar arguments apply in the case of the anti-cut-off diode d_7.

4. CHOICE OF COMPONENTS

Tables I and II gives the important properties of some currently available diodes and transistors which were considered for the circuit. Silicon devices were preferred over germanium ones because of lower leakage currents and higher temperature tolerance.

Switching diodes (d_1, d_2, d_6, d_7) were chosen to be germanium point contact diodes (SEM, Type L). Non-switching diodes, used merely for level shifting (d_3, d_4, d_5), were chosen to be silicon planar diodes (CD 12),

because of their well-defined forward voltage drop. Their large stored charge and high recovery time, as already seen, help in obtaining better speeds.

TABLE I

Transistor characteristics

Transister	P_{max} (mW)	I_{cmax} (mA)	T_{fall} (μs)	T_{sat} (μs)	T_{rise} (μs)	C_{bc} (pf)
2N404 (SEM)	150	100	0·7	0·25	0·7	12
CIL 531 (CIL)	200	100	0·25	0·2	0·20	..
CIL 701 (CIL)	200	200	0·25	0·20	0·20	15

T_{fall}, T_{rise}, and T_{sat} have been measured for I_c = 40 ma and $I_{bf} = I_{br} = 1$ ma.

TABLE II

Diode characteristics

(Recovery times are measured values)

	CD12 (CIL)	CD21 (CIL)	SR100 (CIL)	Type (L) (SEM)	Type (H) (SEM)
1. V_f at I_f = 1ma (V) ..	0·55	0·55	0·20	0·4	0·45
2. V_f at I_f = 5 ma (V) ..	0·65	0·65	0·25	0·65	0·70
3. V_f at I_f = 20 ma (V) ..	0·75	0·75	0·35	0·85	1·20
4. Nonlinearity ..	High	High	Good	Fair	Bad
5. Reverse leakage current at V_6 = 10 V (μa)	1·0	1·0	5·0	10·0	10·0
6. Recovery time at I_f = 3 ma I_b = 3 ma (μs)	1–2	1–2	1–2	·04–·06	·04–·06
7. Reverse breakdown Voltage (V)	12	21	..	20	20

CIL 531 was chosen as the most suitable transistor considering its speed of operation, cost and power dissipation.

5. ENGINEERING AND PERFORMANCE DETAILS

Figure 2 shows a photograph of the module. The way diodes are mounted permits the same basic module to be used for different input configurations.

Table III gives detailed results of the D.C. tolerance analysis performed on the circuit. Margins have been provided between design tolerances and

TABLE III

Results of tolerance analysis

1. Maximum permissible fan-outs	...	8
2. Maximum collector current	...	50 ma
3. Maximum "0" output	...	1·62 V
4. Minimum "1" output	...	5·62 V
5. Maximum permissible "0" input	...	1·86 V
6. Minimum acceptable "1" input	..	3·25 V
7. Maximum power dissipated in transistor	...	90 mW
8. Maximum power consumed per circuit module	...	0·25 W
Parameters assumed for calculations		
1. Maximum allowed fan-ins	...	8 AND inputs, 8 OR inputs
2. Minimum current gain of the transistors	...	45
3. Stray capacity at the output	...	100 pf
4. Typical noise margin	..	0·8 V
5. Variations in the values of resistors and power supplies due to tolerances, aging, wiring, etc.		3·0%

procurement specifications for the various components to ensure system reliability. Figure 3 shows the transfer characteristics of the circuit.

The transient response of the module is shown in Fig. 4.

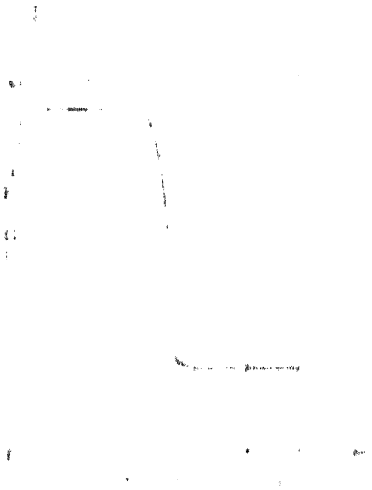

FIG. 3. The transfer characteristics.

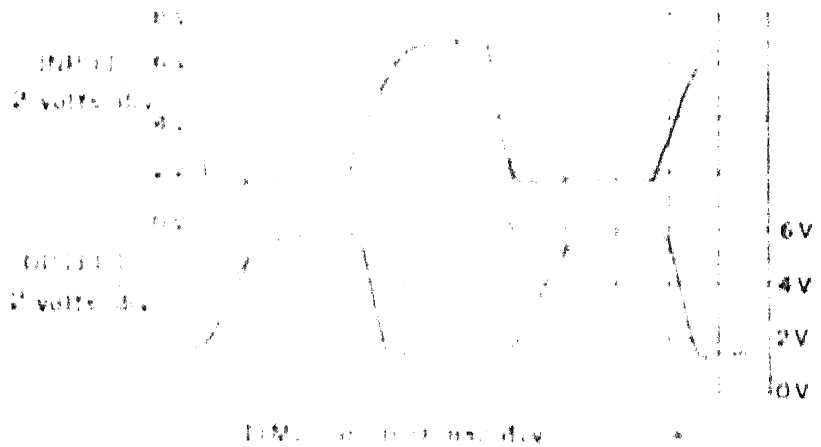

FIG. 4. Transient response of the module

6. Conclusion

The circuit described has been found to work reliably under a wide range of operating conditions, speeds attained compare quite favourably with these attainable using much more expensive devices. The circuit has been so designed as to impose a minimum of limitations on specifications of components; presently used diodes and transistors can be replaced by faster devices of the same general type, with a minimum of redesigning. Noise immunity and operational margins are very adequate for a broad variety of digital equipment.

Information is not yet available about the long range stability of component parameters and their aging characteristics.

7. ACKNOWLEDGMENTS

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REFERENCES

1. Rao, P. V. S. .. "Choice of a digital module for the On Line Data Processor," Technical Memo 2, Computer Centre, T.I.F.R., June 1965.

2. Goldstick, G. H. .. "Comparison of saturated and non-saturated switching circuit techniques," *I.R.E. Transactions on Electronic Computers*, June 1960, **EC-9**, 161–75.

3. Luecke, G. .. "Noise margins in digital integrated circuits," *Proc. I.E.E.E.*, December 1964, **52**, 1565–71.

4. Yao, F. C. .. "Interconnections and noise immunity of circuitry in digital computers," *I.E.E.E. Transaction on Electronic Computesrs*, 1965, pp. 875.

5. ——— .. "Analysis of signal transmission in ultra high speed transistorized digital computers," *Ibid.*, August 1963, **EC-12**, 372–82.

6. Jarvis, D. B. .. "The effects of interconnection on high speed logic circuits," *Ibid.*, October 1963, **EC-12**, 476–87.

7. Gray, H. J. .. *Digital Computer Engineering*, Chapter IX, Prentice-Hall, Englewood Cliffs, 1963.

8. Cho, Y. .. "A method of theoretical analysis of high speed junction diode logic circuits," *I.R.E. Transaction on Electronic Computers*, October 1963, **EC-12**, 492–502.

9. Cagle, W. B., Menne, R. S., Skinner, R. S., Staehler, R. E. and Underwood, M. D. "Logic circuits and their application to the design of the central control," *The Bell System Technical Journal*, September 1964, **43**, 2055–95.

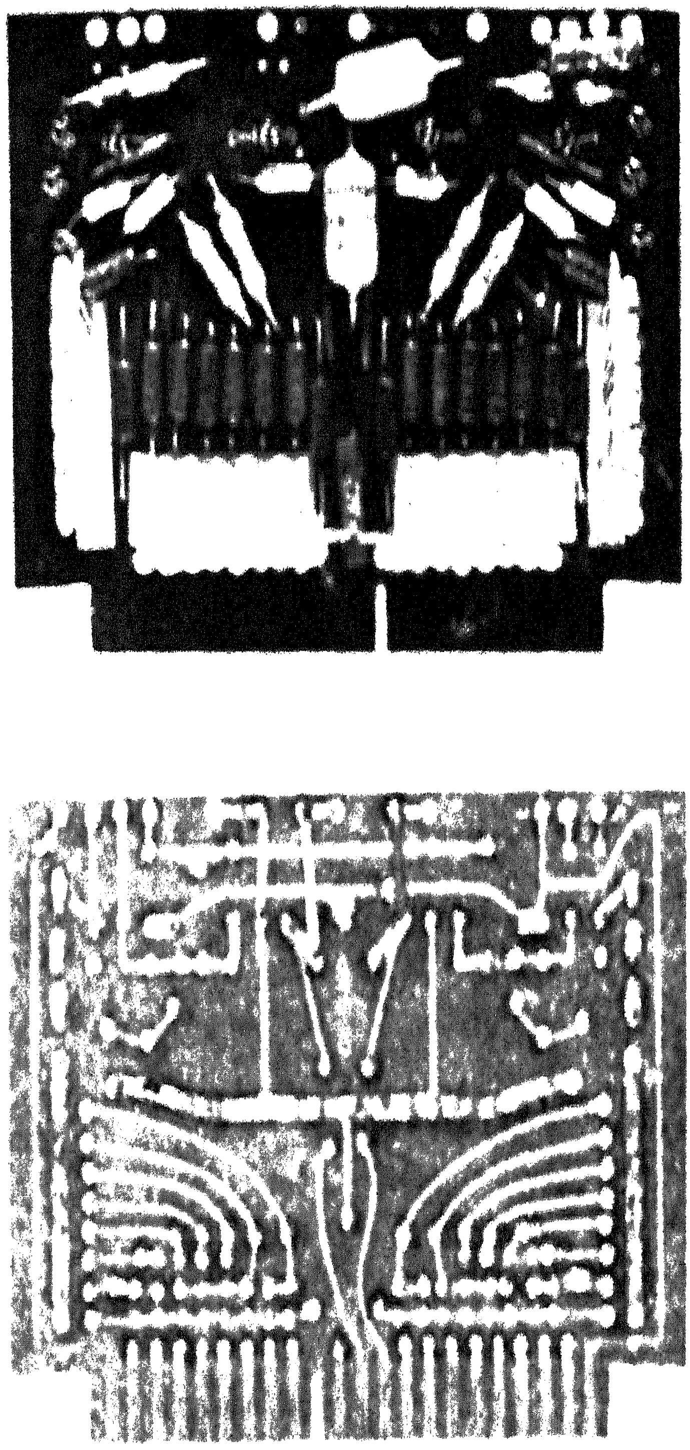

Fig. 2. Top and Bottom Views of Plug-in Card of Line Inverter.