# A Comprehensive Study of Hot-Carrier Induced Interface and Oxide Trap Distributions in MOSFET's Using a Novel Charge Pumping Technique

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***Abstract*—A novel simulation-independent charge pumping (CP) technique is employed to accurately determine the spatial distributions of interface ($N_{it}$) and oxide ($N_{ot}$) traps in hot-carrier stressed MOSFET's. Direct separation of $N_{it}$ and $N_{ot}$ is achieved without using simulation, iteration, or neutralization. Better immunity from measurement noise is achieved by avoiding numerical differentiation of data. The technique is employed to study the temporal buildup of damage profiles for a variety of stress conditions. The nature of the generated damage and trends in its position are qualitatively estimated from the internal electric field distributions obtained from device simulations. The damage distributions are related to the drain current degradation, and well-defined trends are observed with the variations in stress biases and stress time. Results are presented which provide fresh insight into the hot-carrier degradation mechanisms.**

***Index Terms*—Charge pumping, hot-carrier effect, MOSFET, spatial damage profiles.**

## I. Introduction

HOT-CARRIER degradation is one of the key reliability issues encountered in deep submicrometer MOSFET's. The degradation results from a localized and nonuniform buildup of interface states ($N_{it}$) and oxide charges ($N_{ot}$) near the drain junction of the transistor. It manifests itself in the form of threshold voltage shift, transconductance degradation, drain current reduction, etc., and eventually leads to device failure [1]–[3].

To understand and model the degradation, different charge pumping (CP)-based methods have been employed to obtain the spatial distribution of $N_{it}$ and/or $N_{ot}$ created during hot-carrier stressing [4]–[12]. The simulation based methods [4]–[8] employ a source/drain reverse bias [4]–[6] or a variable amplitude gate pulse [7], [8] to vary the CP area and depend heavily on device simulations to determine damage position. These methods are unsatisfactory due to the requirement of exact device structure and doping profiles. The direct methods [9]–[11] employ variable amplitude gate pulse to vary the CP area and calculate the position of the CP edge from prestress measurements on transistors having different gate lengths [12]. Correction to the prestress CP edge for charges associated with the generated defects and the separation of $N_{it}$ and $N_{ot}$ distributions are performed either by neutralization of $N_{ot}$ by a brief carrier injection of the opposite type [9], [10], or by an iterative correction scheme [11]. However it has recently been shown [13] that the existing methods [9]–[12] do not take into account the increase in CP current due to the increased energy zone of recombination (with increased gate pulse amplitude) and hence furnish incorrect CP edges and damage profiles. Moreover, the intermediate carrier injection techniques [9], [10] need separate experimental tools to monitor complete $N_{ot}$ neutralization, and hence in general are complex in nature. On the other hand, the iterative scheme [11], being dependent on repetitive differentiation of experimental data, is highly susceptible to measurement noise and may give rise to convergence problems.

We have recently proposed a new method [14] where the dependence of the CP current on energy zone of recombination is accounted for while calculating the prestress CP edge. By employing both the varying pulse-top and varying pulse-base CP schemes, $N_{it}$ is directly separated from $N_{ot}$ and the prestress CP edge is corrected for generated charges at the interface without using simulation, neutralization, or iteration. A closed-form model, having two independent parameters, is formulated to predict the stress-induced incremental CP current. The model is fitted with experimental data, and the optimized parameter values are used to determine the damage profiles. The method, being immune to measurement noise (since numerical differentiation of the experimental data is avoided), provides robust, accurate distributions of both $N_{it}$ and $N_{ot}$ created during stress.

This paper describes the application of the new method to determine the hot-carrier induced damage creation in n-channel LDD MOSFET's. We have obtained a unique comprehensive set of data on the time evolution of the $N_{it}$ and $N_{ot}$ spatial profiles along the channel for various stress biases. To validate the experimental findings, device simulations using MINIMOS 6.0 were performed. We have found that the nature of the generated damage and trends in its position can be qualitatively estimated from the internal electric field distributions. Finally, the damage distribution is correlated to the device degradation obtained from drain current measurements. The observed device degradation correlates well with the damage profiles and has been found to have well-defined trends with variations in stress time and with gate and drain stress biases.

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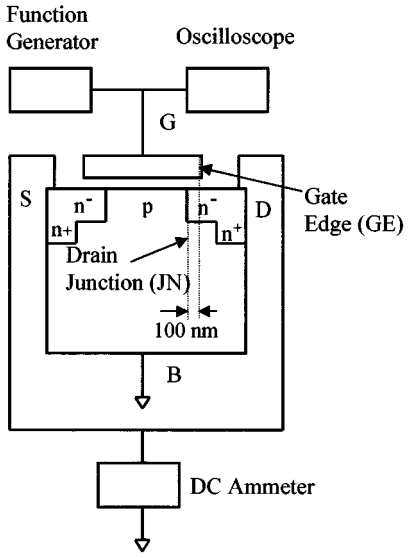


Fig. 1. Charge pumping setup along with the schematic diagram of the MOSFET used in the study showing drain junction (JN), gate-LDD overlap and gate edge (GE).

In Section II of this paper, the new technique is briefly discussed. A fuller account is beyond the scope of the present paper and is presented elsewhere [14], where the correctness, reliability, and robustness of the technique are also demonstrated. Results are presented and discussed in Section III, followed by conclusions in Section IV.

## II. Theory

In charge pumping, the gate of the MOSFET is pulsed from accumulation to inversion using a trapezoidal waveform. The substrate is shorted to ground. The dc current arising out of electron-hole recombination at the interface states is measured at the source and drain, as shown in Fig. 1. The CP measurements are performed both before and after stress in two ways. In the first case, the pulse top level ($V_{\rm top}$) is fixed in inversion ($V_{\rm top} = V_{\rm top,\,max}$) and the pulse base level ($V_{\rm base}$) is varied. The pulse scans the local flatband voltage distribution. In the second case, the pulse base level is fixed in accumulation ($V_{\rm base} = V_{\rm base,\,min}$) and the pulse top level is varied. This pulse scans the local threshold voltage distribution [5].

Assuming a symmetric transistor in prestress and noting the fact that negligible damage takes place in the source half of the channel, the incremental post-stress CP currents as functions of base level and top level of the gate pulse are given by [14]

$$\begin{aligned}\Delta I_{cp}(V_{\rm base}) &= I_{cp,\,s}(V_{\rm base}) - I_{cp,\,v}(V_{\rm base}) \\ &\approx qfW \int_0^{y_{1,\,s}} \Delta N_{it}(y)\,dy \end{aligned} \tag{1}$$

and

$$\begin{aligned}\Delta I_{cp}(V_{\rm top}) &= I_{cp,\,s}(V_{\rm top}) - I_{cp,\,v}(V_{\rm top}) \\ &\approx qfW \int_{y_{1,\,s}}^{y_{m,\,s}} \Delta N_{it}(y)\,dy \end{aligned} \tag{2}$$

where

| | |
|---|---|
| $y = 0$ | chosen at the center of the channel; |
| $\Delta I_{cp}$ | stress-induced incremental CP current; |
| $I_{cp,\,v}$, $I_{cp,\,s}$ | measured currents, respectively, in the virgin and stressed conditions; |
| $q$ | electronic charge; |
| $f$ | frequency of the gate pulse; |
| $W$ | width of the transistor; |
| $\Delta N_{it}(y)$ | generated interface-state density at $y$. |

The edge $(y_{1,\,s})$ of the CP zone in the post-stress case is defined for the varying base-level measurements as $V_{FB,\,s}(y_{1,\,s}) = V_{\rm base}$, and for the varying top-level measurements as $V_{T,\,s}(y_{1,\,s}) = V_{\rm top}$, where $V_{FB,\,s}$ and $V_{T,\,s}$ are, respectively, the local flatband and threshold voltage distributions in the post-stress case. The maximum CP edge $(y_{m,\,s})$ in post-stress corresponding to $V_{\rm base,\,min}$ is defined by $V_{FB,\,s}(y_{m,\,s}) = V_{\rm base,\,min}$. Note that (1) and (2) satisfy the relation

$$\begin{aligned}&\Delta I_{cp}(V_{\rm top}) + \Delta I_{cp}(V_{\rm base}) \\ &\quad = \Delta I_{cp,\,\max}(V_{\rm top,\,max},\, V_{\rm base,\,min}) \\ &\quad = qfW \int_0^{y_{m,\,s}} \Delta N_{it}(y)\,dy \end{aligned} \tag{3}$$

so that for a given value of $V_{\rm base}$ and hence $\Delta I_{cp}$ in post-stress, the corresponding value $V_{\rm top}$ can be obtained from (3). We will discuss this later in the section.

For MOSFET's with thin gate oxides, the generated interface-state density profile can be modeled by an analytically integrable function close to a Gaussian in shape as [14]

$$\Delta N_{it}(y) = \frac{\Delta N_{it,\,p}(y)}{\cosh^2 \alpha(y - y_p)} \tag{4}$$

where

| | |
|---|---|
| $\Delta N_{it,\,p}$ | peak value of damage; |
| $y_p$ | position of the peak along the channel; |
| $\alpha$ | parameter whose reciprocal is a measure of the spatial spread of the damage. |

Using (4) in (1) and by assuming that the contribution to the total incremental CP current by the interface-states generated in the source half of the channel is negligible, one obtains

$$\begin{aligned}\frac{\Delta I_{cp}(V_{\rm base})}{qfW} &= \int_0^{y_{1,\,s}} \Delta N_{it}(y)\,dy \approx \int_{-\infty}^{y_{1,\,s}} \Delta N_{it}(y)\,dy \\ &= \frac{\Delta N_{it,\,p}}{\alpha}\left[1 + \tanh\,\alpha(y_{1,\,s} - y_p)\right] \end{aligned} \tag{5a}$$

and for the maximum incremental CP current

$$\Delta I_{cp,\,\max}(V_{\rm top,\,max},\, V_{\rm base,\,min}) = qfW\frac{\Delta N_{it,\,p}}{\alpha}\left[1+\beta\right] \tag{5b}$$

where $\beta$ is defined by the relation

$$\beta = \tanh\,\alpha(y_{m,\,s} - y_p). \tag{5c}$$

Using (5a) and (5b), one obtains, after some simple manipulations,

$$y_{1,\,s} = y_{m,\,s} - \frac{1}{2\alpha}\,\ln\left[\frac{2 - (1+\beta)x}{1 - \beta x}\right] \tag{6}$$

where $x$ is given by $x = \Delta I_{cp}/\Delta I_{cp,\,\max}$.

Now, note that in the post-stress case, $V_{T,s}(y_{1,s}) = V_{\text{top}}$ and $V_{FB,s}(y_{1,s}) = V_{\text{base}}$. Therefore the post-stress local $V_{T,s}$ and $V_{FB,s}$ values at any point $y_{1,s}$ in the channel are related to the prestress ones by [14]

$$V_{\text{top}} - V_{\text{base}} = V_{T,v}(y_{1,s}) - V_{FB,v}(y_{1,s}) + \frac{q\Delta N_{it}(y_{1,s})}{C_{ox}} \quad (7)$$

where $V_{T,v}$ and $V_{FB,v}$ are the prestress local threshold and flatband voltage distributions (as obtained later), $C_{ox}$ is the oxide capacitance per unit area. Note that by using (7), the $\Delta N_{ot}$ term is automatically removed. Putting (6) in (4) and putting all together in (7), one obtains

$$V_{\text{top}} - V_{\text{base}} = f_{VTFB}(y_{1,s}) + \frac{q}{C_{ox}} \frac{\alpha \Delta I_{cp,\max}}{qfW} \cdot [2 - (1+\beta)x]x \quad (8)$$

where $f_{VTFB}$ is a polynomial function fitted through the prestress $V_{T,v} - V_{FB,v}$ versus $y$ data and $y_{1,s}$ is given by (6).

For all $V_{\text{base}}$ and hence $\Delta I_{cp}$ value in post-stress, the corresponding $V_{\text{top}}$ is obtained from (3). Equation (8) is fitted with the experimental $V_{\text{top}} - V_{\text{base}}$ versus $\Delta I_{cp}/\Delta I_{cp,\max}$ data and the two unknown parameters, namely $\alpha$ and $\beta$ are obtained. The parameter $\Delta N_{it,p}$ is obtained from (5b), while $y_p$ is obtained from (5c). Once the parameters $\alpha$ and $\beta$ are obtained, for each of the $V_{\text{base}}$ (and hence $\Delta I_{cp}$) values in post-stress, the CP edge $y_{1,s}$ is obtained from (6). Since $V_{FB,s}(y_{1,s}) = V_{\text{base}}$ at $y_{1,s}$, $V_{FB,s}$ is known. Again, from the prestress $V_{FB} - y$ relation, for $y_{1,s}$, $V_{FB,v}$ is also known. Therefore $\Delta N_{ot}$ can be obtained from

$$V_{\text{base}} = V_{FB,v}(y_{1,s}) - \frac{q\Delta N_{ot}(y_{1,s})}{C_{ox}} - \frac{q\Delta N_{it}(y_{1,s})}{2C_{ox}} \quad (9)$$

since the $\Delta N_{it}$ values are already obtained using (4). Note that the data fitting and the subsequent analysis to obtain the $N_{it}$ and $N_{ot}$ distributions has to be performed separately for each stress conditions having different gate and drain bias and stress time.

Now, to obtain the $V_{FB,v} - y$ relation in prestress, the CP current can be rewritten as [13]

$$\frac{I_{cp,v}(V_{\text{base}})}{2qfW} = \langle N_{it,v}(V_{\text{base}}) \rangle \left[ \frac{Ld}{2} - \Delta y_{1,v}(V_{\text{base}}) \right] \quad (10)$$

where

- $\Delta y_{1,v}$ zone excluded from CP and is related to the CP edge ($y_{1,v}$) by the relation $y_{1,v}(V_{\text{base}}) = L_d/2 - \Delta y_{1,v}(V_{\text{base}})$;
- $y_{1,v}$ edge of the CP zone in prestress and is given by $V_{FB,v}(y_{1,v}) = V_{\text{base}}$;
- $\langle N_{it,v}(V_{\text{base}}) \rangle$ spatial average of $N_{it}(y)$ up to $y_{1,v}$;
- $L_d$ drawn gate length.

While $y_{1,v}(V_{\text{base}})$ is dependent on the drawn gate length, $\Delta y_{1,v}(V_{\text{base}})$ is not. Therefore, $(1/2)I_{cp,v}(V_{\text{base}})$ (measured on transistors of different $L_d$ but identical otherwise) is plotted as a function of $L_d/2$. The data points are fitted with a straight line. The intercept of the fitted straight line gives $\Delta y_{1,v}$ and hence $y_{1,v}$ [13]. This process is repeated for all $V_{\text{base}}$ values to obtain $y_{1,v}$ as a function of $V_{\text{base}}$, which is essentially the prestress $V_{FB,v} - y$ relation. In a similar manner, the prestress $1/2(I_{cp,v}(V_{base,\max}) - I_{cp,v}(V_{\text{top}}))$ data is plotted versus $L_d/2$. The intercepts of the fitted straight lines through the data points drawn for all $V_{\text{top}}$ values furnishes the $V_{T,v} - y$ relation [14].

Finally, we discuss the determination of the maximum CP edge ($y_{m,s}$) in the post-stress case. As discussed before, $y_{m,s}$ (corresponding to $V_{\text{base,min}}$) is defined by $V_{FB,s}(y_{m,s}) = V_{\text{base,min}}$. A similar relation in prestress relating $y_{m,v}$ and $V_{FB,v}$ is $V_{FB,v}(y_{m,v}) = V_{\text{base,min}}$ where $V_{FB,v}$ and $y_{m,v}$ are the local flatband voltage distribution and the maximum value of the CP edge, respectively, in the prestress case. Since $V_{FB,v}$ depends only on device doping, for a given $V_{\text{base,min}}$ value, $y_{m,v}$ is constant (w.r.t channel-LDD junction) for devices having different drawn gate lengths but identical otherwise. On the other hand, $V_{FB,s}$ is different from $V_{FB,v}$ due to charges associated with the generated defects, and therefore $y_{m,s}$ is dependent on stress conditions. However, it is assumed that for $y_{m,s}$ deep inside the junction (for large $|V_{\text{base,min}}|$ value), the $N_{it}$ and $N_{ot}$ generated at $y_{m,s}$ are small to make any appreciable change in the local flatband voltage distribution. Therefore, the condition $V_{FB,v}(y_{m,v}) = V_{FB,s}(y_{m,s}) = V_{\text{base,min}}$ is satisfied, which implies $y_{m,v} = y_{m,s}$ and hence $y_{m,s}$ can be determined from prestress $V_{FB,v} - y$ relation as obtained above.

## III. Results and Discussion

Charge pumping measurements using the method discussed above were carried out on submicrometer LDD MOSFET's as shown in Fig. 1. The gate of the MOSFET is pulsed using a trapezoidal waveform obtained from an HP33120A function generator. The CP current is measured at the source and drain using a Keithley 617 electrometer, preceeded by an LC low-pass filter. The substrate is shorted to ground. Measurements were performed using gate pulses having a frequency of 1 MHz with rise and fall time of 250 ns. For the varying base-level measurements, the pulse top level was fixed at $V_{\text{top,max}} = 1$ V. For the varying top-level measurements, the pulse base level was fixed at $V_{\text{base,min}} = -4$ V. Experiments were performed using isolated LDD n-channel MOSFET's having 0.8–0.25 μm effective channel lengths ($L_{\text{eff}}$), oxide thickness ($T_{ox}$) of 11 nm, and gate width of 10 μm. The stress induced damage distributions and the resulting drain current degradation are shown for the transistor having $L_{\text{eff}} = 0.3$ μm. The devices have a gate-LDD overlap of 100 nm, as shown in Fig. 1. Note that for a given gate and drain bias, the stress measurements for different times are performed on the same transistor. However, the stressing at different gate and drain voltages are performed on different transistors located on different (but adjacent) dies in the wafer.

In Fig. 2, the prestress $V_{T,v}$ and $V_{FB,v}$ distributions are plotted along the channel (left $y$ axis) for a device having $L_{\text{eff}} = 0.3$ μm. These results are obtained from the prestress $I_{cp,v} - V_{\text{top}}$ and $I_{cp,v} - V_{\text{base}}$ measurements performed on transistors having different drawn gate lengths as described in the previous section. Note that corresponding to $V_{\text{base,min}} = -4$ V, the maximum CP edge in prestress is $y_{m,v} = 50$ nm (w.r.t the channel LDD junction) and is situated in the gate-LDD overlap region. Also shown (right $y$ axis) is the prestress $V_{T,v} - V_{FB,v}$ value along the channel for the same transistor. The $V_{T,v} - V_{FB,v}$ versus $y$ data is fitted with a polynomial $f_{VTFB}$ (solid line) and is used in (8), which is finally used for fitting the experimental data. The

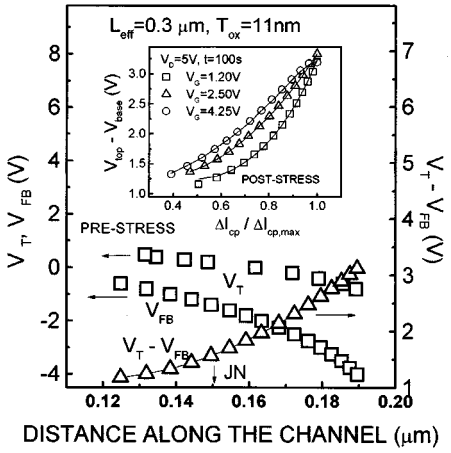


Fig. 2. Prestress $V_{T,\,v}$, $V_{FB,\,v}$ (left $y$ axis) and $V_{T,\,v} - V_{FB,\,v}$ (right $y$ axis) distribution along the channel. (Inset) Calculated (solid line) and experimental (symbols) $V_{\rm top} - V_{\rm base}$ versus $\Delta I_{cp}/\Delta I_{cp,\,\max}$ plot. The stressings were done at $V_G = 1.2$, 2.5, and 4.25 V, $V_D = 5$ V for $t = 100$ s.

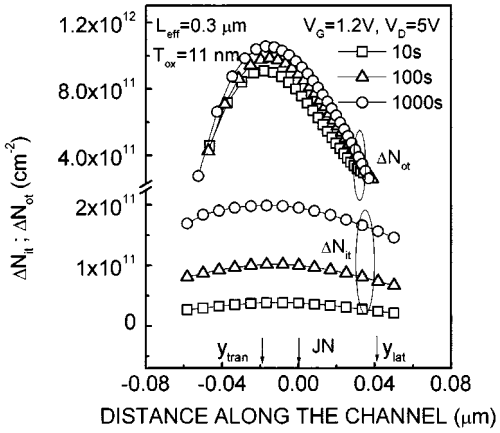


Fig. 3. Interface-state density ($\Delta N_{it}$) and oxide trapped charge density ($\Delta N_{ot}$) profiles along the channel as a function of stress time. Stressing was done at $V_G = 1.2$ V, $V_D = 5$ V. The origin is chosen at the drain junction (JN), and the gate edge is at 0.1 μm. The quantities $y_{lat}$ and $y_{tran}$ are defined in the text of Fig. 6.

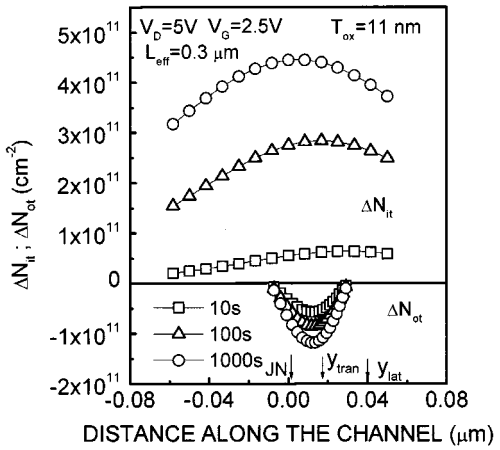


Fig. 4. Interface-state density ($\Delta N_{it}$) and oxide trapped charge density ($\Delta N_{ot}$) profiles along the channel as a function of stress time. Stressing was done at $V_G = 2.5$ V, $V_D = 5$ V. The origin is chosen at the drain junction (JN), and the gate edge is at 0.1 μm. The quantities $y_{lat}$ and $y_{tran}$ are defined in the text of Fig. 6.

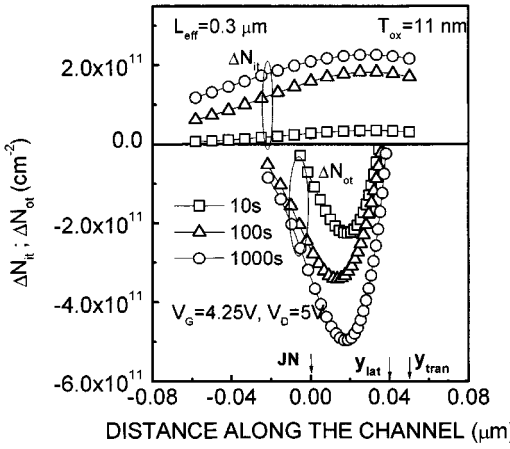


Fig. 5. Interface-state density ($\Delta N_{it}$) and oxide trapped charge density ($\Delta N_{ot}$) profiles along the channel as a function of stress time. Stressing was done at $V_G = 4.25$ V, $V_D = 5$ V. The origin is chosen at the drain junction (JN), and the gate edge is at 0.1 μm. The quantities $y_{lat}$ and $y_{tran}$ are defined in the text of Fig. 6.

inset shows post-stress $V_{\rm top} - V_{\rm base}$ versus $\Delta I_{cp}/\Delta I_{cp,\,\max}$ data as obtained from (3). Stressing was performed at $V_D = 5$ V. The gate voltages were 1.2, 2.5, and 4.25 V and the stress time was 100 s. The symbols are experimental data points, and the solid lines are the model fit, performed separately for each stress case using (8). As can be seen the model fits the experimental data extremely well. The model parameters $\alpha$ and $\beta$ are extracted from such fits, for each stress bias and time.

In Figs. 3–5, the stress induced $\Delta N_{it}$ and $\Delta N_{ot}$ profiles are plotted along the channel. The origin ($y = 0$) of these figures are chosen at the channel-LDD junction. The stressing was done at $V_D = 5$ V for 10, 100, and 1000 s. The gate voltages were 1.2 V (Fig. 3), 2.5 V (Fig. 4), and 4.25 V (Fig. 5). It can be seen that with increase in stressing time, the $\Delta N_{it}$ and $\Delta N_{ot}$ distributions increase both in magnitude and in spread. For all the different stress conditions, the peak position of $\Delta N_{it}$ and $\Delta N_{ot}$ distribution correlates well, lying within a distance of 15 nm of each other. For stressing at low $V_G$, the damage peaks are slightly away from the junction. However, for stressing at high $V_G$, the damage is observed mostly inside the gate-LDD overlap region. $\Delta N_{it}$ is generated at all $V_G$ values, the maximum being at $V_G = 2.5$ V, which is also the condition for maximum substrate current measured during stressing. Hole trapping is observed for stressing at $V_G = 1.2$ V, while electron trapping is observed for the other two stress conditions (plotted on a negative scale), the maximum being at $V_G = 4.25$ V. For our devices, we observe more hole trapping (which saturates at longer times) than electron trapping. Similar $V_G$ dependence of the damage distributions are observed on other devices having different gate lengths and oxide thicknesses.

The qualitative nature of the generated damage and its position as a function of gate bias during stressing are compared with electric field profiles obtained from MINIMOS 6.0 simulations. The device dopings are obtained from SUPREM 4 simulations. The simulated lateral ($E_{lat}$) and the transverse ($E_{tran}$) electric field profiles along the channel are shown in Fig. 6 for $V_D = 5$ V and $V_G = 1.2$, 2.5, and 4.25 V. As can be seen, for $V_D = 5$ V, the position ($y_{lat}$) of the $E_{lat}$ peak is situated in the gate-LDD overlap

region at 35 nm from the drain junction, and is found to be almost independent of $V_G$. On the other hand the position $y_{tran}$ where $E_{tran}$ changes sign is a strong function of $V_G$. For $V_G = 1.2$ V, $y_{tran}$ is situated to the left of $y_{lat}$, at −15 nm from the junction. The negative $E_{tran}$ between $y_{tran}$ and $y_{lat}$ assists in large hole injection, resulting in dominant hole trapping near the junction (see Fig. 3). For $V_G = 4.25$ V, $y_{tran}$ is situated at the right of $y_{lat}$ at 55 nm from the junction. The positive $E_{tran}$ between $y_{tran}$ and $y_{lat}$ assists in large electron injection, resulting in dominant electron trapping in the gate-LDD overlap region (see Fig. 5). As can be seen from Fig. 6, the portion of the channel where $E_{tran}$ is positive for $V_G = 1.2$ V (and conducive for electron injection) and negative for $V_G = 4.25$ V (and conducive for hole injection) are far away from $y_{lat}$. Therefore for such cases either fewer electrons or holes are injected into the oxide and hence the generated interface states are less, which conforms to the trapped-hole recombination model [15]. The peak of the generated interface traps is near the drain junction for $V_G = 1.2$ V and in the gate-LDD overlap region for $V_G = 4.25$ V, consistent with position of $y_{tran}$ with respect to $y_{lat}$ for such stress conditions. Finally for $V_G = 2.5$ V, $y_{tran}$ is at 20 nm from the junction and is situated close to $y_{lat}$. Therefore, both holes and electrons are injected in large quantities, resulting in large interface trap generation and no significant charge trapping (see Fig. 4). Note that $y_{tran}$ and the position of the interface-state density peak for $V_G = 2.5$ V are situated midway between that at $V_G = 1.2$ V and at $V_G = 4.25$ V. Also note that due to the larger capture cross-section of the hole traps and low hole mobility in the oxide, the existing hole traps are rapidly filled during the initial period of stressing and thus acts as a limiting factor for further hole trapping. On the contrary, electron trapping is a less rapid process due to the higher electron mobility and lower capture cross-section of electron traps. Also electron trapping is observed at high $V_G$ values where $E_{tran}$ is also higher, which results in field assisted detrapping of trapped electrons. Therefore, trapped electrons are lower in magnitude than trapped holes and does not show saturation.

In Fig. 7, the interface-state density peak ($\Delta N_{it,p}$), spread ($\Delta\sigma$), the differential peak transconductance ($\Delta g_m/g_{m,o}$) (left $y$ axis) and the measured substrate current ($I_{sub}$) during stress (right $y$ axis) are plotted as a function of stress $V_G$. The stressing was performed at $V_D = 5$ V for 500 s. The transconductance is calculated from the $I_D - V_G$ characteristics measured at $V_D = 0.1$ V both before and after stress. $\Delta\sigma$ is defined as the length of the channel where the condition $\Delta N_{it} \geq N_{it,c}$ is satisfied, where $N_{it,c}$ is a chosen cut-off value. Mathematically, $\Delta\sigma$ is given by $\cosh(\Delta\sigma/2) = (\Delta N_{it,p}/N_{it,c})^{1/2}$. We have chosen the cut-off value as $N_{it,c} = 5 \times 10^{10}$ cm$^{-2}$. Note that this choice of $N_{it,c}$ is somewhat arbitrary and a different value of $N_{it,c}$ would result in a different value of $\Delta\sigma$. However, we have found that the trends in $\Delta\sigma$ as functions of gate and drain bias and stress time is independent of the choice of $N_{it,c}$. Therefore, once a value of $\Delta N_{it,c}$ is chosen, it can be used to have a comparative estimate of the damage spread for various stress biases and times, and all our arguments which is based entirely on the damage trends remains unaffected by the choice of $N_{it,c}$.

It can be seen from Fig. 7 that $\Delta N_{it,p}$ is maximum in the region where $V_G \approx V_D/2$. $\Delta\sigma$ shows a local maximum at $V_G$ values slightly less than the $V_G = V_D/2$ condition. Note that

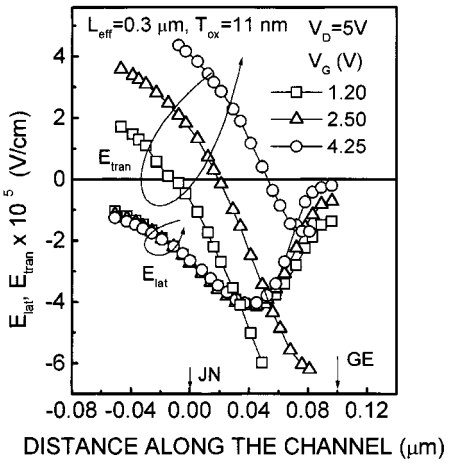


Fig. 6. Simulated lateral and transverse electric field profiles along the channel for a transistor having $L_{\rm eff} = 0.3$ μm and $T_{ox} = 11$ nm, for $V_D = 5$ V and $V_G = 1.2$, 2.5, and 4.25 V.

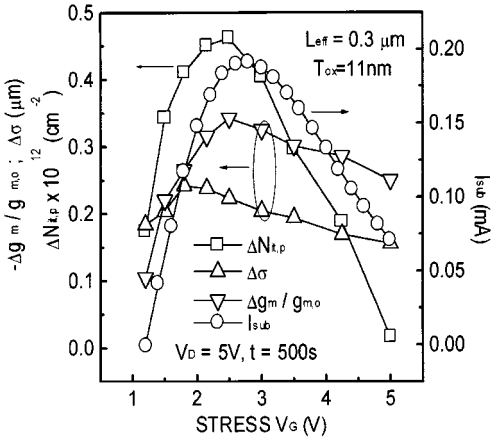


Fig. 7. Interface-state density peak magnitude ($\Delta N_{it,p}$), spread ($\Delta\sigma$), normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$) (left $y$ axis) and substrate current ($I_{sub}$) measured during stress (right $y$ axis) as a function of stress gate voltage. Stressing was done at $V_D = 5$ V for 500 s.

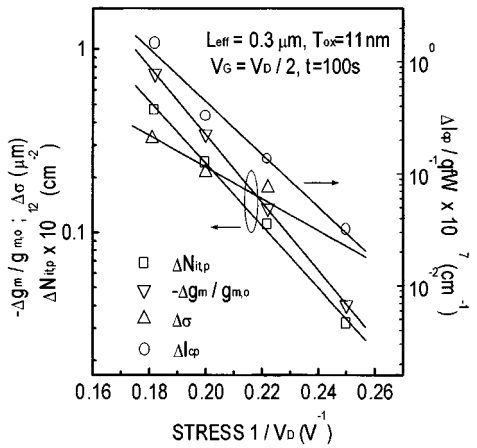


Fig. 8. Interface-state density peak magnitude ($\Delta N_{it,p}$), spread ($\Delta\sigma$), normalized peak transconductance degradation ($\Delta g_m/g_{m,o}$) (left $y$ axis) and incremental CP current ($\Delta I_{cp}/qfW$) (right $y$ axis) as a function of stress drain voltage. Stressing was done at $V_G = V_D/2$ for 100 s.

contrary to the $\Delta N_{it,p} - V_G$ relation, the overall $\Delta\sigma - V_G$ trend does not quite follow the $I_{sub} - V_G$ trend. The $\Delta g_m - V_G$ relation follows the $\Delta N_{it,p} - V_G$ pattern for low $V_G$ values, and

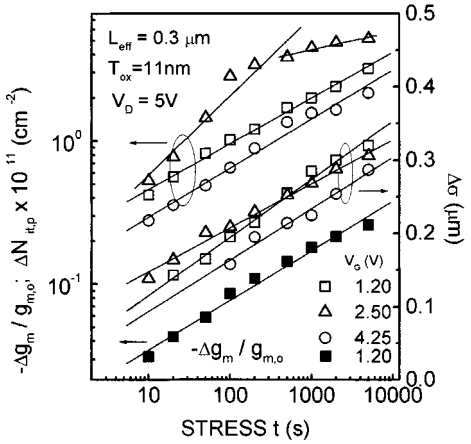


Fig. 9. Buildup of interface-state density peak ($\Delta N_{it,p}$), (left $y$ axis) and spread ($\Delta\sigma$), (right $y$ axis) versus time for different gate voltage during stress. Also shown the normalized peak transconductance ($\Delta g_m/g_{m,o}$) for stressing at $V_G = 1.2$ V (left $y$ axis). The stress $V_D$ was 5 V.

is maximum near $V_G = V_D/2$. However for $V_G > V_D/2$, $\Delta g_m$ decreases slightly and follows the $\Delta\sigma - V_G$ trend. Note that for stressing at low $V_G$'s, the interface-trap peak is situated near the channel-LDD junction (Fig. 3) and therefore has a strong impact on transconductance degradation. However for stressing at high $V_G$'s the peak of interface trap moves inside the gate-LDD overlap region (Fig. 5). Therefore, transconductance degradation will be affected more by the interface traps situated in the channel region estimated by the spread. This implies that both the magnitude and spread of the interface-state density profile are separately responsible for $g_m$ degradation, each contributing to a larger or lesser degree depending on the bias condition.

In Fig. 8, $\Delta N_{it,p}$, $\Delta\sigma$, $\Delta g_m/g_{m,o}$ (left $y$ axis) and $\Delta I_{cp}/qfW$ (right $y$ axis) are plotted as a function of stress $V_D$. The gate voltage was held at $V_G = V_D/2$ for all values $V_D$, and the stress time was 100 s. It can be seen that $\Delta I_{cp}$, $\Delta N_{it,p}$, $\Delta\sigma$ and thus $\Delta g_m$ increase with $V_D$ and follow an $\exp(-a/V_D)$ dependence. With increase in $V_D$, the increase in $\Delta N_{it,p}$ ($a_1 = 39.13$ V) is higher than the increase of $\Delta\sigma$ ($a_2 = 13.08$ V). As expected, the slope of $\Delta I_{cp}$ ($a_3 = 54.1$ V) is close to that of $\Delta N_{it,p}, \Delta\sigma$ ($a_1 + a_2 = 52.21$ V). $\Delta g_m$ has a higher slope ($a_4 = 42.64$ V) than $\Delta N_{it,p}$, and the difference is due to the increase in $\Delta\sigma$ with $V_D$. This verifies that both the peak and the spread of the generated interface traps are responsible for $g_m$ degradation. However note that $a_1 + a_2 \neq a_4$, which implies that $\Delta g_m$ depends nonlinearly on $\Delta N_{it,p}$ and $\Delta\sigma$. This nonlinearity can be attributed to the fact that the peak of generated interface traps is in the gate-LDD overlap region, and interface traps situated in the overlap region do not affect the transconductance as strongly as the traps situated in the channel region as estimated by the spread.

In Fig. 9, $\Delta N_{it,p}$ (log scale, left $y$ axis) and $\Delta\sigma$ (linear scale, right $y$ axis) are plotted as a function of stress time (log scale). The stress $V_G$'s were 1.2, 2.5, and 4.25 V, and the stress $V_D$ was fixed at 5 V. Also shown is $\Delta g_m$ for stressing at $V_G = 1.2$ V on a log scale (left $y$ axis). It can be seen that $\Delta N_{it,p}$ follows a strong $t^n$ variation with distinct values of $n$ for different stress $V_G$'s . For the present device, we observe $n = 0.32$, 0.55 and 0.34 for $V_G = 1.2$, 2.5, and 4.25 V, respectively. Both the magnitude and rate of $\Delta N_{it,p}$ buildup is maximum for stressing at $V_G = 2.5$ V, which however shows a saturation for larger times. The time evolution of $\Delta\sigma$ shows a slower rate and goes as $A\log(t)$. The rate of increase of $\Delta\sigma$ is maximum for stressing at $V_G = 1.2$ V. The value of $A$ is 0.08 ($V_G = 1.2$ V) and 0.05 ($V_G = 2.5$ and 4.25 V) μm/decade. No saturation is observed in $\Delta\sigma$ buildup for larger times. These trends are also observed on devices having different channel length and oxide thicknesses. $\Delta g_m$ shows the well known $t^n$ dependence with time, with $n = 0.35$ for $V_G = 1.2$ V (plotted) and $n = 0.58$ and 0.36 for $V_G = 2.5$ and 4.25 V (not shown) respectively, similar to the published results [3]. Once again, the higher slope of $\Delta g_m$ as compared to $\Delta N_{it,p}$ can be attributed to the increase in $\Delta\sigma$ with time. These observations confirm the fact that both the peak and spread of the generated interface trap profiles are responsible for $g_m$ degradation.

## IV. Conclusion

To summarize, a novel CP technique is employed to obtain the interface ($N_{it}$) and oxide ($N_{ot}$) trap distributions in hot-carrier stressed MOSFET's. The new technique does not require computer simulation, neutralization, or iteration, is inherently immune to measurement noise and directly provide separate $N_{it}$ and $N_{ot}$ profiles along the channel. We have obtained an unique comprehensive set of data on damage distributions as a function of stress time for various stress biases. It has been found that hole trapping near the drain junction and electron trapping in the gate-LDD overlap region are the dominant degradation modes respectively at low and high gate biases. Interface traps are created for all stress conditions, the maximum being at medium gate biases. The nature and position of the generated defects correlate well with the lateral and transverse field distributions as obtained from device simulations, and it has been shown that both electrons and holes are required in the oxide for the creation of interface traps. Both $N_{it}$ and $N_{ot}$ profiles increase in magnitude and in spread with increased stress time, though the increase in magnitude is more compared to the spread. Finally the observed $g_m$ degradation is found to be dependent on both the peak magnitude and spread of the generated interface traps. The $g_m$ degradation follow the trends observed in interface trap formation with variations in stress gate and drain biases, and stressing times. This study therefore provides fresh insight into the hot-carrier degradation mechanisms.

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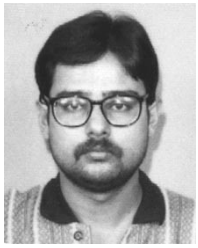
## References

[1] K. R. Hofmann, C. Wener, W. Weber, and G. Dorda, "Hot-electron and hole-emmision effects in short n-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-32, p. 691, 1985.

[2] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 2194, 1988.

[3] G. Groeseneken, R. Bellens, G. Van den bosch, and H. E. Maes, "Hot-carrier degradation in submicrometer MOSFET's: From uniform injection toward the real operating conditions," *Semicond. Sci. Technol.*, vol. 10, p. 1028, 1995.

[4] M. G. Ancona, N. S. Saks, and D. McCarthy, "Lateral distributions of hot-carrier induced interface traps in MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 2221, 1988.
[5] W. Chen, A. Q. Balasinski, and T. P. Ma, "Lateral profiling of oxide charge and interface traps near MOSFET junctions," *IEEE Trans. Electron Devices*, vol. 40, p. 187, 1993.
[6] H.-H. Li, Y.-L. Chu, and C.-Y. Wu, "A novel charge pumping method for extracting the lateral distributions of interface traps and effective oxide charge densities in MOSFET devices," *IEEE Trans. Electron Devices*, vol. 44, p. 782, 1997.
[7] R. G.-H. Lee, J.-S. Su, and S. S. Chung, "A new method for characterizing the spatial distributions of interface states and oxide-trapped charges in LDD n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 43, p. 81, 1996.
[8] R. G.-H. Lee, J.-P. Wu, and S. S. Chung, "An efficient method for characterizing time-evolutional interface state and its correlation with the device degradation in LDD n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 43, p. 898, 1996.
[9] C. Chen and T. P. Ma, "Direct lateral profiling of both interface traps and oxide charge in thin gate MOSFET devices," in *Tech. Dig., Symp. VLSI Tech.*, 1996, p. 230.
[10] D. S. Ang and C. H. Ling, "A novel experimental technique for the lateral profiling of oxide and interface state charge in hot-hole degraded n-MOSFET's," *IEEE Electron Device Lett.*, vol. 19, p. 23, 1998.
[11] W. K. Chim, S. E. Leang, and D. S. H. Chan, "Extraction of metal-oxide-semiconductor field-effect-transistor interface state and trapped charge spatial distributions using a physics-based algorithm," *J. Appl. Phys.*, vol. 81, p. 1992, 1997.
[12] M. Tsuchiaki, H. Hara, T. Morimoto, and H. Iwai, "A new charge pumping method for determining the spatial distribution of hot-carrier induced fixed charge in p-MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, p. 1768, 1993.
[13] S. Mahapatra, C. D. Parikh, and J. Vasi, "A new "multifrequency" charge pumping technique to profile hot-carrier induced interface-state density in n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 46, p. 960, 1999.
[14] S. Mahapatra, C. D. Parikh, J. Vasi, V. Ramgopal Rao, and C. R. Viswanathan, "A direct charge pumping technique for spatial profiling of hot-carrier induced interface and oxide traps in MOSFET's," *Solid-State Electron*, vol. 43, p. 915, 1999.
[15] S. K. Lai, "Two-carrier nature of interface-state generation in hole trapping and radiation damage," *Appl. Phys. Lett.*, vol. 39, p. 58, 1981.



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