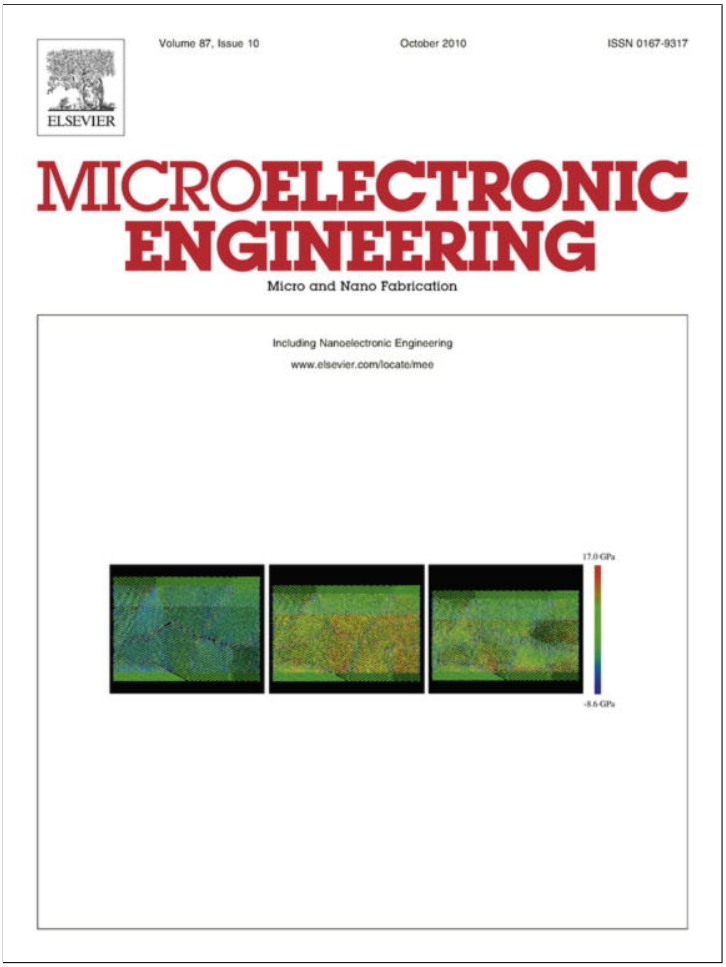

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Implications of fin width scaling on variability and reliability of high-k metal gate FinFETs

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ABSTRACT

In this paper, we report a study to understand the fin width dependence on performance, variability and reliability of n-type and p-type triple-gate fin field effect transistors (FinFETs) with high-k dielectric and metal gate. Our results indicate that with decreasing fin width the well-known performance improvement in terms of sub-threshold swing and drain-induced barrier lowering are accompanied by a degradation of the variability and the reliability. As a matter of fact fin width scaling causes (i) higher hot-carrier degradation (HC) in nFinFETs owing to the higher charge carrier temperature for the same internal stress voltages; (ii) worse negative bias temperature instability (NBTI) in pFinFETs due to the increased contribution from the (1 1 0) surface; (iii) higher variability due to the non-uniform fin extension doping, as highlighted by applying a novel characterization technique.

1. Introduction

For the past few decades Moore's Law has become the guiding force for CMOS scaling [1]. As the MOSFET is shrunk down, the gate controllability of the channel potential decreases due to a high longitudinal field from the drain, resulting in enhanced short-channel effects (SCEs). Multi-gate MOSFETs (MuGFETs) have been considered to be promising candidates for future scaling of CMOS technologies into the sub 32 nm node. A variety of multi-gate device architectures are currently being investigated including the Planar Double Gate, FinFET, Tri-Gate or Gate-all-around structures [2–4]. Due to their 3D architecture a number of geometrical parameters are involved in MuGFET optimization thus making the MuGFET design a very challenging task. In particular, one of the fundamental geometrical parameters of FinFET is its patterned fin width, which needs to be smaller than the gate length for acceptable short channel performance [5]. Several papers have analyzed the performance dependence on fin width by means of simulations and measurements. It is well known that sub-threshold swing (SS) and drain-induced barrier lowering (DIBL) improve in narrow nFinFETs [6,7]. On the other hand, it has been shown that parasitic source/drain (S/D) resistance increases by decreasing the fin width and that the Selective Epitaxial Growth (SEG) of Si on the S/D-HDD regions is a potential solution for minimizing the parasitic S/D resistance of narrow fin devices [8,9]. Also a few works have addressed the implications of fin width scaling on variability and reliability. Xion and Bokor [10] studied through Monte Carlo simulations the impact of variations of geometrical parameters such as gate length, fin width, oxide thickness etc. on the SCEs and they showed that variation in fin width is the most important parameter to control from the overall device variation point of view. Lee et al. studied negative bias temperature instability (NBTI) in pFinFETs with standard SiO_2 gate dielectric and observed a higher degradation in narrow fins [11].

However, there has so far been no systematic experimental study to understand the dependence of performance, variability and reliability on the fin width in FinFET devices. This work essentially addresses this aspect for the case of n-type and p-type silicon on insulator (SOI) triple-gate FinFETs with high-k and metal gate. A novel characterization technique for doping profile variation along the fin height is also proposed.

2. Experimental details

The experiments were performed on SOI FinFETs with fin height of 60 nm, fin length of 50 nm (except for the mobility measurements where we used FinFETs with length of 10 μm), fin width varying from 25 to 75 nm, bulk oxide thickness (t_{BOX}) of 145 nm and background doping of 10^{15} cm^{-3}. Fin corner rounding was em-

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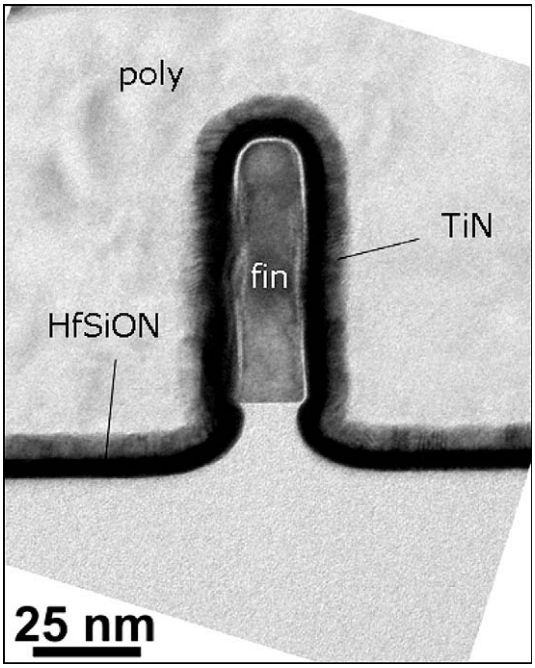

Fig. 1. A cross sectional TEM image of the fin after gate patterning.

ployed using H_2 annealing, followed by ALD deposition of HfSiON (50%) and PVD deposition of TiN metal electrode. Equivalent oxide thickness (EOT) is about 1.9 nm. Gate stack deposition was then followed by source/drain extension implant, spacer formation, HDD implants and nickel silicidation. Fig. 1 is a TEM image of the fin after gate patterning. The device electrical characterization was done using a Keithley 4200 semiconductor characterization system and an HP4284 LCR meter. All measurements were done at room temperature unless stated otherwise. Mobility data have been extracted by using the split CV technique.

3. Results and discussion

3.1. Performance

The devices show ON currents (V_{OV} = 1 V, V_{DS} = 1.2 V) up to 1.5 mA/μm and OFF currents (V_{GS} = 0 V, V_{DS} = 1.2 V) of 2 nA/μm as shown in Fig. 2 [12]. A significant improvement in SS and DIBL is obtained by decreasing the fin width for both types of FinFETs, as reported in Fig. 3. Values as low as 67 mV/dec were observed

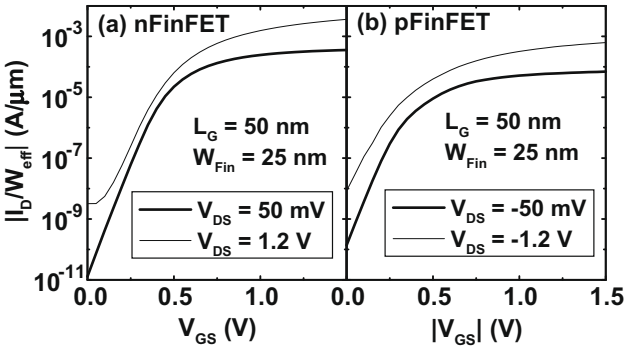

Fig. 2. I_D–V_{GS} characteristics of nFinFETs and pFinFETs with L_G = 50 nm and W_{Fin} = 25 nm at low and high V_{DS}. I_D is normalized by effective fin width (W_{eff} = 2H + W_{Fin}).

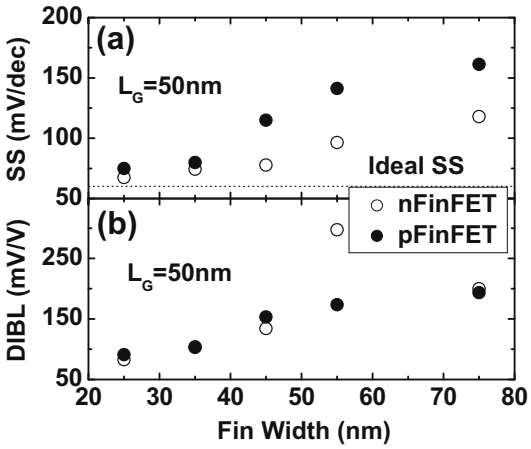

Fig. 3. (a) Sub-threshold swing and (b) DIBL as a function of fin width for nFinFET and pFinFET devices with L_G = 50 nm. Significant improvements are observed in narrow fins.

for SS, which can be attributed to low doping levels in the fin and to the better gate control in these devices. Close to ideal values for SS and acceptable short channel performance can be achieved by scaling the fins down to 25 nm [13].

The fractional contribution of (1 0 0) plane gets modified with fin width. While the electron mobility is higher on the (1 0 0) surface in comparison to the (1 1 0) one, the hole mobility has the opposite trend. As a result, increasing the fin width, the overall carrier mobility enhances for nFinFETs and decreases for pFinFETs (Fig. 4). It is worth noting that the absolute change in mobility is more evident in nFinFETs than the pFinFETs. Furthermore we can observe that the strong mobility variation in nFinFET at low inversion charge densities can be mainly ascribed to a change in the coulomb and phonon scattering rates.

3.2. Variability

Fig. 5 shows the I_D–V_G curves of nFinFET with gate length L_G = 50 nm, fin width W_{Fin} = 25 nm and fin height H_{Fin} = 60 nm, biased with V_{DS} = 50 mV and V_{BG} swept from −40 V to +40 V. It can be seen that I_D–V_G curve shows a strong dependence on the back gate bias for V_G values greater than V_T [14]. This implies that with increased negative value of V_{BG}, the S/D series resistance R_{SD} is modulated owing to the depletion of bottom portion of the doped fin region. Fig. 6(a) shows one half of the fin extension re-

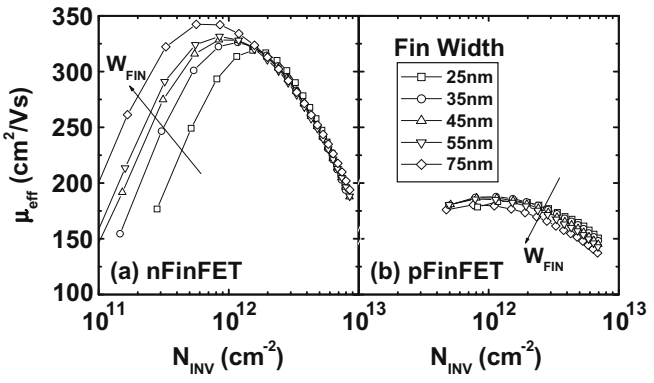

Fig. 4. Effective carrier mobilities as a function of inversion carrier density for different fin widths. Due to different mobility behaviours of electrons and holes in (1 0 0) and (1 1 0) planes, the overall carrier mobility decreases for narrow nFinFETs and slightly increases for narrow pFinFETs.

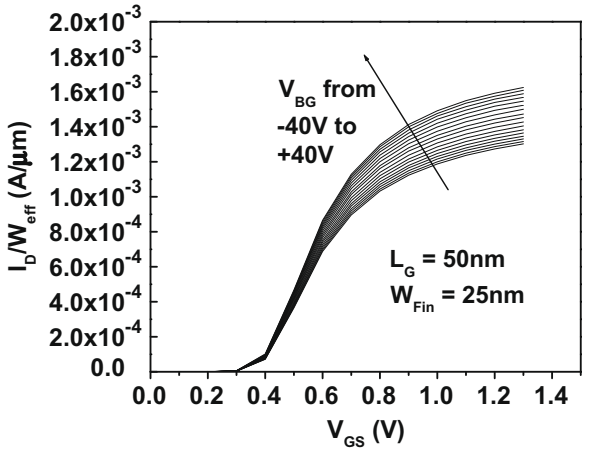

Fig. 5. I_D–V_G measurement of nFinFET with L_G = 50 nm, W_{Fin} = 25 nm and H_{Fin} = 60 nm, showing the sensitivity of I_{ON} on the back gate voltage (−40 V to +40 V) with t_{BOX} = 145 nm.

gion of the FinFET device (which is the region of importance here). When the back gate voltage is negative, the bottom portion of the fin region gets depleted. This actually affects the S/D series resistance and modulates the drain current. Full 3D process and device simulations have been carried out to study this effect in detail using the calibrated TCAD tool set [15–17]. Fig. 6(b) shows the 3D view showing the bottom depletion, validating our hypothesis. The extension region with the BOX constitutes a structure very similar to the MOS capacitor. Here the influence of V_{DS} is minimal as measurement is taken at V_{DS} = 50 mV. Using a first order model for the depleted region, (as shown in Fig. 6(a)) we can get the following equation

$$\frac{R_{SD-MIN}}{R_{SD}(V_{BG})} = 1 - \frac{h_D(V_{BG})}{H_{Fin}} \tag{1}$$

where h_D is the height of the depleted bottom portion of the extension region, R_{SD-MIN} is the minimum S/D resistance when there is no depletion in the fin extensions. In the depletion approximation we can write the following expression

$$V_{BG} = V_{fb} + \Psi_S + \frac{\sqrt{2\varepsilon_s q N_a \Psi_S}}{C_{BOX}} \tag{2}$$

Eliminating Ψ_s from Eq. (2) in terms of h_D, and subsequently differentiating it, we get

$$N_a = \frac{1}{q\left(\frac{h_D}{\varepsilon_s} + \frac{1}{C_{BOX}}\right)\left(\frac{dh_D}{dV_{BG}}\right)} \tag{3}$$

where N_a is the average doping in the depletion width corresponding to a voltage V_{BG} By plotting the N_a at different values of h_D (i.e. corresponding to different V_{BG}), which are very closely packed, we can get an estimate of the actual bottom doping profile. The method is sufficient enough to characterize the bottom fin doping, which is crucial in real devices as the fin extension top portion will always be more heavily doped. This illustrates that this method can be easily used to characterize the bottom fin doping from simple I_D–V_G measurements. The method can be extended to any arbitrary doping profiles such as Gaussian, by suitably modifying the Eq. (2). For any arbitrary doping profile where no closed form solution for ψ_S is available, the same method can be applied by numerically solving the equations. The extracted doping profiles along the height of the fin (from the bottom fin region) are shown in Fig. 7. Here we can see that the extension region doping depends on the fin width and it shows a significant variation along the height of the fin for narrower fins. The non-uniformity can be particularly important for the matching performance of FinFETs. The variability induced by the channel doping is expected to be very low because of low doping in the fin. In Fig. 8, we show how the relative standard deviation in I_{ON}, for the set of 10 devices, depends on the fin width. In particular, the variability of FinFET devices increases when the fin width approaches around 40 nm. This experimental observation is in agreement with the results shown in Ref. [18]. Several works

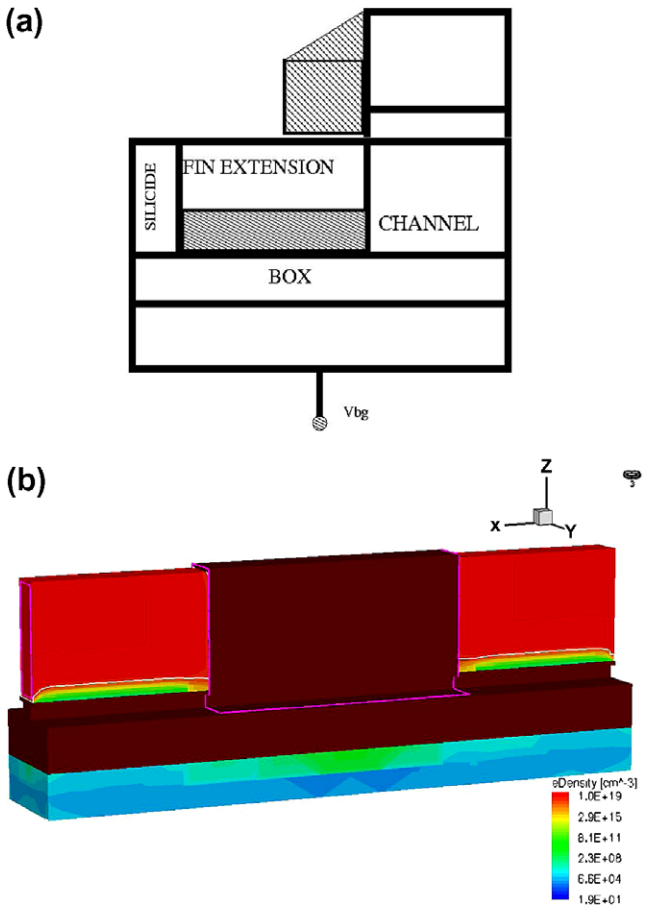

Fig. 6. (a) Cross section of one half of the FinFET (including extension region) showing the depletion of fin extension, due to back gate. (b) 3D perspective view of the carrier distribution in the FinFET structure at V_{BG} = −40 V showing the depletion of carriers in the bottom of fin.

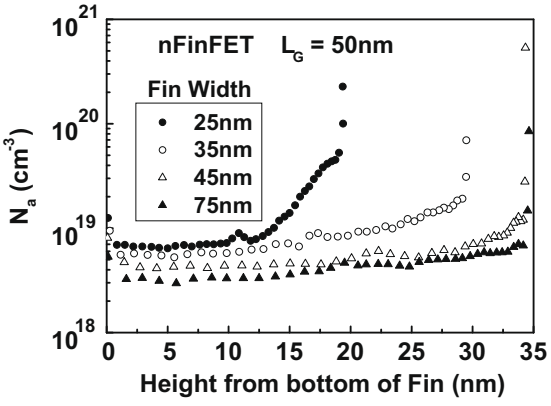

Fig. 7. Fin extension doping profile as a function of height from the bottom of fin for different fin widths. Doping profile shows significant variation along the height of the fin for narrower fins.

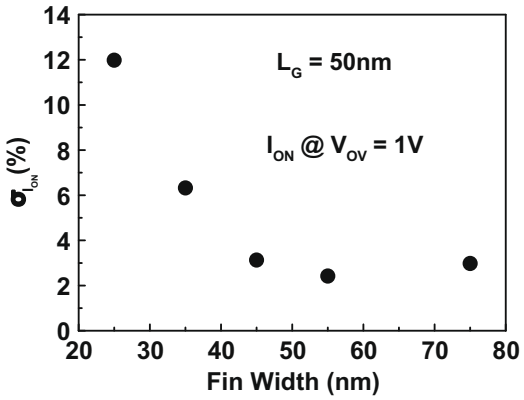

Fig. 8. Percentage standard deviation in ON current versus fin width for the devices with $L_G = 50$ nm. ON current measured at $V_{OV} = 1$ V and $V_{DS} = 1.2$ V. Narrow fin shows higher I_{ON} variability due to non-uniformity in the extension region.

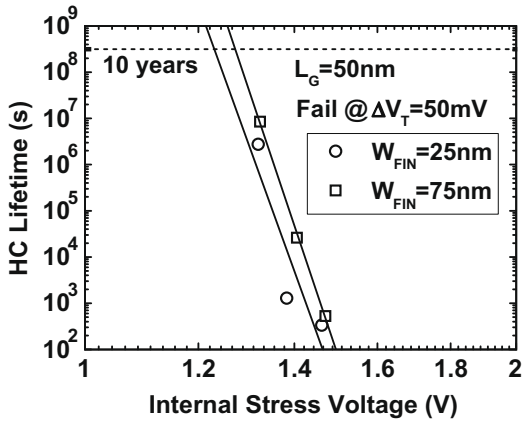

Fig. 10. Extracted lifetime for HC stress condition $V_{Gint} = V_{Dint}$ as a function of stress voltage for different fin widths. Narrow fins show worse HC lifetime.

[18,19] have shown how the line width roughness can become the main source of variability in FinFET devices where the channel is lowly doped and the fin width is extremely reduced. However, based on the previous doping profile study, the higher I_{ON} variability observed for the narrow fin could be partially attributed to the non-uniformity in the extension region.

3.3. Reliability

A smaller hot-carrier (HC) degradation is observed in nFinFETs with narrow fins stressed at $V_G = V_D$ (see Fig. 9). A question arises as to whether this improvement in HC lifetime is real due to an intrinsic higher robustness against HC or it is apparent due to the higher S/D series resistance [8,9]. In order to answer to this question, we repeated the HC measurements for the same values of the internal gate and drain voltages $V_{Gint} = V_{Dint}$:

$$\begin{cases} V_{Gint} = V_G - \frac{R_{SD}}{2} I_D \\ V_{Dint} = V_D - R_{SD} I_D \end{cases} \quad (4)$$

where R_{SD} is the sum of the source and the drain series resistances, which have been assumed equals. As shown in Fig. 10, once we remove the effects of S/D series resistance, the opposite trend is observed. To understand this experimental observation, we performed 2D Medici device simulations of double gate nMOSFETs with physical characteristics similar to the triple-gate device used in experiments. Although the use of 2D simulations cannot reproduce well the impact of corner injection in triple-gate devices, we preferred to keep the analysis simple in order to obtain a qualitative comparison with experiments. The simulated structures have an SiO_2 gate oxide thickness of 1.9 nm, a body doping of 10^{15} cm^{-3}, a gate length of 50 nm and different fin widths ranging from 20 nm to 80 nm. The simulated gate current, calculated through the Lucky Electron Model, and the maximum electron temperature along the channel are plotted in Fig. 11. The higher gate injection for thinner fin width is caused by the higher electron temperature at the drain side and a reduced effective barrier height. Due to the reduced short-channel effects for thinner fin width, the potential can vary in a shorter region close to the drain, which causes a higher maximum electric field and a higher maximum carrier temperature. Let us note that the device is fully depleted because of the low bulk doping, so that a thinner width causes a lower gate oxide voltage drop and a lower injection field. Simulation and experiments show that this effect is negligible with respect to the higher electron temperature which causes a higher HC degradation.

A larger NBTI degradation is observed in pFinFETs with narrow fins (see Figs. 12 and 13). A similar result has been already reported for pFinFETs with standard SiO_2 gate dielectric by Lee et al. [11], thus suggesting that the NBTI worsening in narrow fins is not related to a particular type of gate stack. Results shown in Figs. 12 and 13 are consistent with the fact that the sidewall channel of

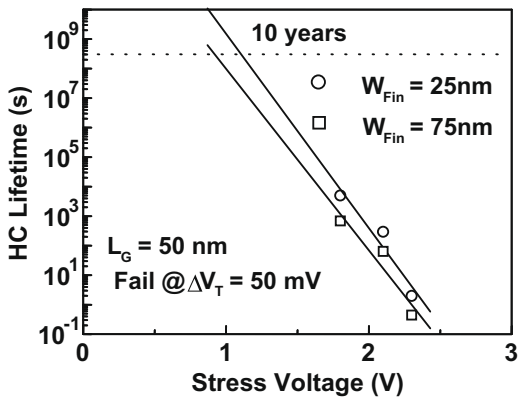

Fig. 9. Extracted lifetime for HC stress condition $V_G = V_D$ as a function of stress voltage for different fin widths. Narrow fins show improved HC lifetime.

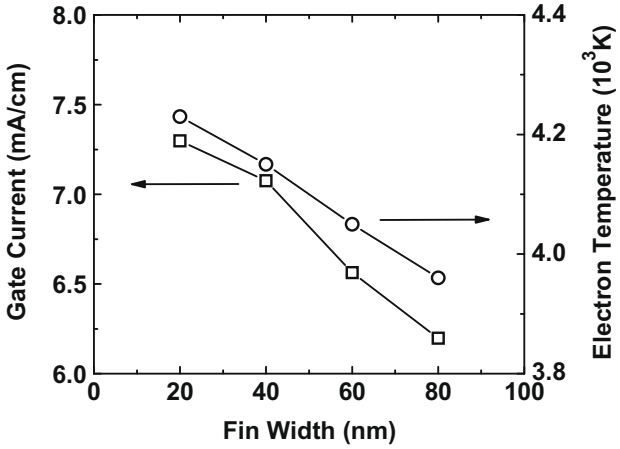

Fig. 11. Simulated gate current (left axis) and electron temperature (right axis) by 2D Medici device simulations. The simulated structures have a SiO_2 gate oxide thickness of 1.9 nm, a body doping of 10^{15} cm^{-3}, a gate length of 50 nm and different fin widths ranging from 20 nm to 80 nm. For narrow fins the gate injection increases due to the higher electron temperature.

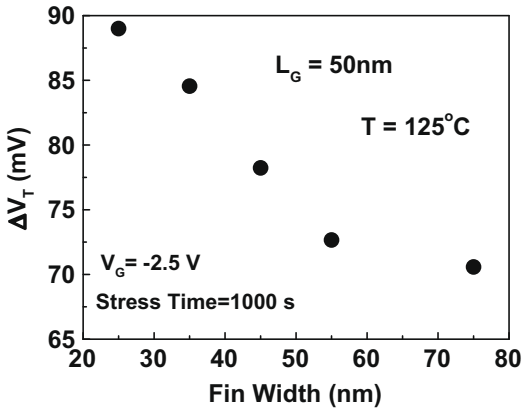

Fig. 12. Threshold voltage shift after stressing pFinFET at V_G = 2.5 V, 125 °C for 1000 s as a function of fin width.

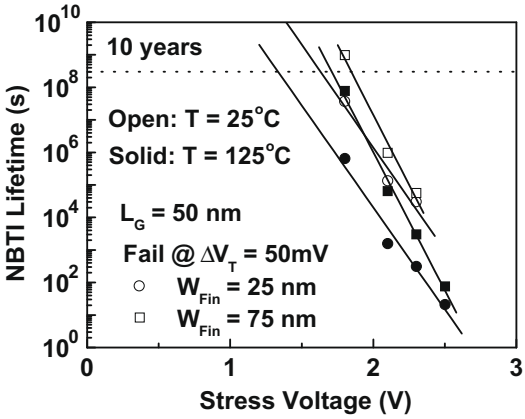

Fig. 13. Extracted NBTI lifetime as a function of stress voltage at 25 °C and 125 °C for different fin widths. Narrow fins show worse NBTI lifetime.

(1 1 0) Si surface has more dangling bonds and it is therefore expected that there is a higher concentration of bonded hydrogen after passivation at this interface as compared to the (1 0 0) top-side orientation [20]. Moreover, as suggested in [11], the larger NBTI in narrow fins can be also caused by the higher hole concentration at the interface between the fin and the gate dielectric.

4. Conclusion

We reported a study of the implications of the fin width scaling on performance, variability and reliability in n-type and p-type SOI triple-gate FinFETs with high-k and metal gate. This work shows that with decreasing fin width the well-known performance improvement in terms of sub-threshold swing and drain-induced barrier lowering are accompanied by a degradation of the variability and the reliability. Fin width scaling negatively affects the variability due to the non-uniform doping profile of the fin extension regions, as highlighted with a novel characterization technique. We have shown that the apparent higher robustness against HC observed in narrow nFinFETs for the same applied external stress voltages is due to a higher series resistance. Once we remove the effects of the series resistance by applying the same internal stress voltages, the opposite trend is observed. This observation is ascribed to the higher charge carrier temperature in narrow fins as confirmed by numerical 2D simulations. NBTI in pFinFETs gets worse with decreasing fin width, owing to the relative contributions from the (1 0 0) and the (1 1 0) planes and to the increased hole concentration at the interface between the fin and the gate dielectric. These drawbacks could ultimately limit the fin width scaling, which is a very important consideration from the device design point of view.

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