Low Temperature-High Pressure Grown Thin Gate Dielectrics for MOS Applications

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In this study we propose high pressure grown oxide (HIPOX) as an alternative low-temperature MOS gate insulator and show that it performs excellently in comparison to other widely reported low-temperature deposited oxides. Our optimized process conditions for HIPOX result in high quality gate dielectric comparable in quality to the standard thermal dry oxide in terms of initial properties as well as under various stress conditions. Sub 100 nm channel length vertical MOSFETs with HIPOX as a gate dielectric are fabricated and characterized to demonstrate the suitability of HIPOX as a low-temperature MOS gate dielectric.

1. INTRODUCTION

Reduced thermal budget processing of deep sub-micron MOSFETs and thin film technologies have brought about increased interest in low-temperature oxides. Much of the low-temperature oxide study has however been concentrated on the deposited oxides with a wide variety of annealing conditions, generally a high temperature anneal to improve the quality of the oxide [1]-[5]. In this work we report for the first time high-pressure grown oxide (HIPOX) as an alternative MOS gate dielectric and compare its performance with the deposited oxides. However, one of the main factors limiting VLSI device reliability is the degradation caused by hot carriers. These hot carriers are known to cause interface state generation, electron trapping at the Si/SiO_2 interface and also charge trapping in the oxide bulk [6]-[10]. For these reasons, not only must any SiO_2 dielectric possess good initial quality, but should also perform well under accelerated stress conditions. For this reason, we have looked at the high-field performance of all these different oxides, namely: low-pressure chemical vapor deposited (LPCVD) oxide, remote plasma enhanced chemical vapor deposited (RPECVD) oxide and finally, the high pressure pyrogenic steam grown oxide (HIPOX) and compared their degradation characteristics with the standard thermally grown dry oxide under different stress conditions. Finally, vertical MOSFETs with channel lengths below 100 nm are fabricated using HIPOX as the gate dielectric to demonstrate the suitability of HIPOX for low-temperature MOS applications.

2. EXPERIMENTAL CONDITIONS

For the initial optimization of all the gate oxides, extensive work has been done on poly-silicon gate MOS capacitors with all the above gate oxides, namely: LPCVD oxide, RPECVD oxide, HIPOX and the thermal dry oxide. The thermal dry oxide is used as the control oxide. The MOS capacitors (of area 0.04×10^{-2} cm^2) used in this study were fabricated on 4" p-type (100) Si substrates using standard polysilicon gate technology. The control SiO_2 was thermally grown in O_2 at 800^0 C. LPCVD oxide deposition was done at 420^0 C using silane and oxygen reaction while for the remote plasma enhanced SiO_2, the substrate temperature was 300^0 C and the deposition was done using tetraethylorthosilane (TEOS) and oxygen. High-pressure oxidation was carried out at 650^0C in a commercial high-pressure

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oxidation reactor in pyrogenic steam at a pressure of 10^5 Pa using O_2. The oxide thickness for all the types of oxides was 10 nm. An anneal at 750° C was given for all the oxides to a total time of 40 minutes in N_2/O_2 as a densification step. This anneal temperature was chosen based on our simulation and experimental results on MOSFETs with channel lengths of 150 nm, which show that oxidation temperatures above 750° C would cause thermal out-diffusion of dopants making the devices dysfunctional [11]. Except for the gate insulator growth process, all other processing conditions were kept the same for all the wafers. The above optimized process conditions for all the oxides are summarized in Table 1 and the measured initial characteristics on poly-silicon gate MOS capacitors are shown in Table 2. The excellent initial properties of all these oxides shows the effectiveness of the process optimization done for these oxides.

For all the high-field stress experiments, the capacitors were stressed by a constant current. The configuration used for constant current stressing consisted of a Keithley 220 current source and a Keithley 617 electrometer, which was used to monitor the voltage across the capacitor. The stress current was interrupted at regular intervals to monitor the degradation. HF-LF CV technique was used for the measurement of midgap interface state density (ΔD_{itm}) and the midgap voltage shift (ΔV_{mg}). Experiments were performed by injecting charge from the metal as well as from the substrate. For the experiments where silicon was the injecting electrode, the devices were exposed to light of sufficient quantity such that the injection was not limited by the rate of generation of minority carriers.

Type of Oxide	Oxidation Parameters
Thermal dry	T=800°C, Dry oxidation in O_2
HIPOX	T=650°C, P= 10 bar
LPCVD Oxide	T=420°C, reactive gases SiH_4 and O_2. Ratio between SiH_4 to O_2 is 1:5. Pressure: 35 Pa
Remote PECVD Oxide	T=300°C, TEOS process

Table 1: Optimized process conditions for various gate dielectrics.

Type of Oxide	V_{fb} (V)	D_{itm} (eV^{-1}. cm^{-2})	Q_{BD} (coul. cm^{-2})	T_{ox} variation across Wafer (%)
Thermal Dry	-0.87	$1.3x10^{10}$	> 50	2
Remote PECVD oxide	-0.86	$1.5x10^{10}$	12.5	7
LPCVD oxide	-0.86	$1.9x10^{10}$	10	10
HIPOX	-0.87	$9x10^{9}$	> 50	9

Table 2: Measured characteristics on the virgin poly Si gate MOS capacitors with various dielectrics.

3. ELECTRICAL CHARACTERIZATION

The initial I-V characteristics are shown in Fig. 1 and the breakdown field distribution is shown in Fig. 2 for all the optimized 10nm gate oxide capacitors with different gate dielectrics. Constant current injection experiments were also carried out on all these different gate oxides to assess their hot-carrier reliability. Figure 3 shows the ΔV_{mg} in all these oxides as a function of stress time for two different current densities. As can be seen, deposited oxides show electron trapping while the HIPOX and thermal oxides show conventional hole trapping. The excess Si-H and Si-OH centers in deposited oxides are known to act as electron trap centers [9]. HIPOX, as can be seen, shows shifts comparable to that of a thermal dry oxide.

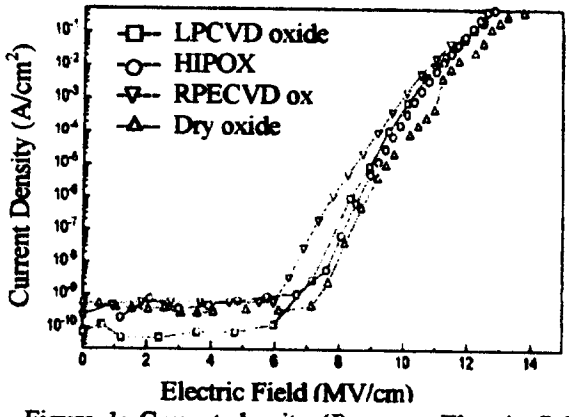

Figure 1: Current density (J) versus Electric field (E) for different oxides in accumulation.

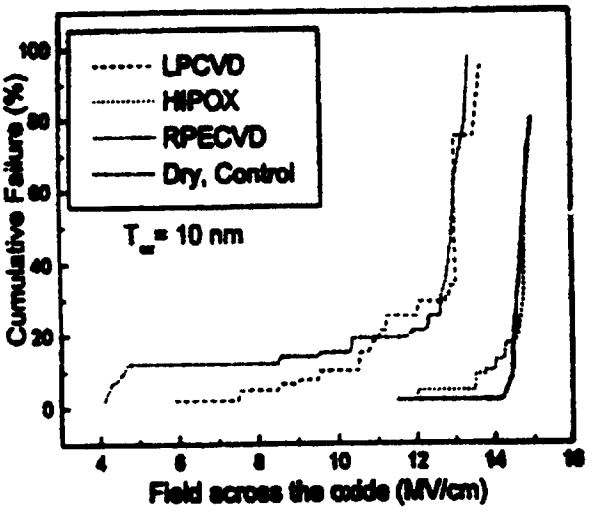

Figure 2: Breakdown field distribution in various gate oxide capacitors.

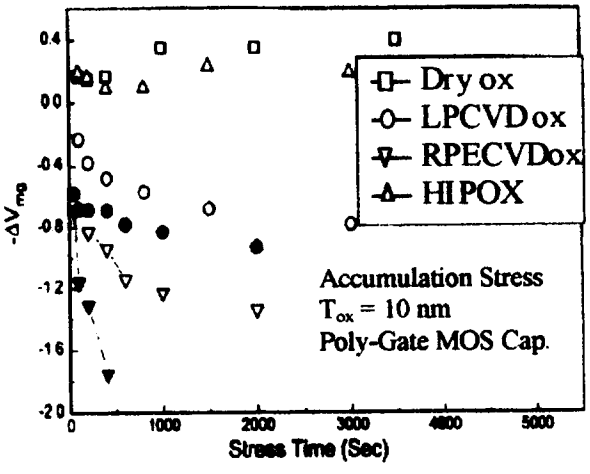

Figure 3: Midgap voltage shifts (ΔV_{mg}) as a function of stress time for various oxide capacitors. Open symbols are for a stress current of 0.25 mA/cm^2 and filled symbols are for corresponding oxides (LPCVD and RPECVD ox) at a stress current of 2.5 mA/cm^2.

The change in gate voltage during constant current stress in all the four types of oxides is shown in Fig 4. The higher trapping rate in RPECVD oxides as observed from the larger change in V_G during the constant current stress is also responsible for the low Q_{BD} values observed in these oxides. We also observe a good correlation between Q_{BD} and ΔV_G in this work. In general, oxides with lower Q_{BD} show higher ΔV_G during constant current stress. The stress induced mid-gap interface state generation (ΔD_{itm}) is shown in Fig 5. In LPCVD oxides, it can be seen that there is an order of magnitude higher ΔD_{itm} compared to HIPOX for identical stress conditions. RPECVD oxides are much worse compared to even the LPCVD oxides and are therefore not shown.

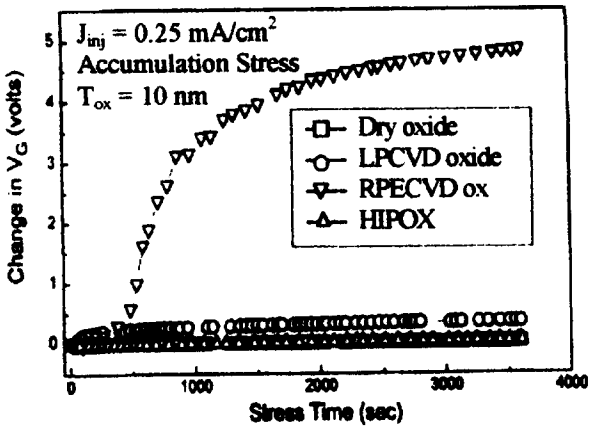

Figure 4: Change in gate voltage (ΔV_G) during constant current injection.

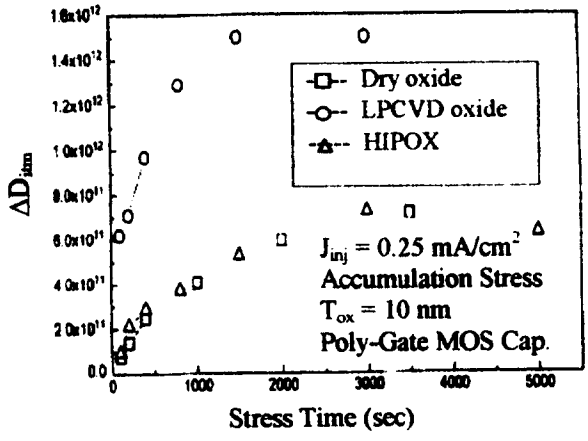

Figure 5: Change in mid-gap interface state density as a function of stress time.

In order to demonstrate the applicability of HIPOX as a MOS gate dielectric, vertical sub 100nm Si MOSFETs are fabricated using HIPOX as the gate dielectric. The schematic of the vertical MOSFET structure with gate oxide surrounding the mesa is shown in Fig. 6 (a) while the fabricated MOSFET structure is shown in Fig. 6 (b). HIPOX is used as a gate dielectric with a thickness of 14nm. HIPOX was grown at 600°C at P=10 bar in

pyrogenic steam without any additional high-temperature anneal. The gate oxide thickness of 14nm was chosen mainly to avoid corner breakdown at the mesa edges. The detailed process sequence for these vertical MOSFETs is reported elsewhere [12]. Measured input characteristics are shown in Fig. 7 [12]. The measured value of low-field mobility in these MOSFETs is 420cm^2/V-s indicating a good HIPOX/Si interface. This excellent low-field mobility has also been recently shown to give rise to high velocity overshoot effects in these vertical MOSFETs [13].

4. CONCLUSIONS

High-pressure grown oxide is optimized to exhibit excellent characteristics as a MOS gate dielectric. Vertical sub 100nm channel length MOSFETs employing the optimized low-temperature HIPOX are fabricated and shown to exhibit excellent mobility and I-V characteristics.

ACKNOWLEDGEMENTS

This work has been carried out under the sandwich model fellowship offered by the German Academic Exchange Service (DAAD).

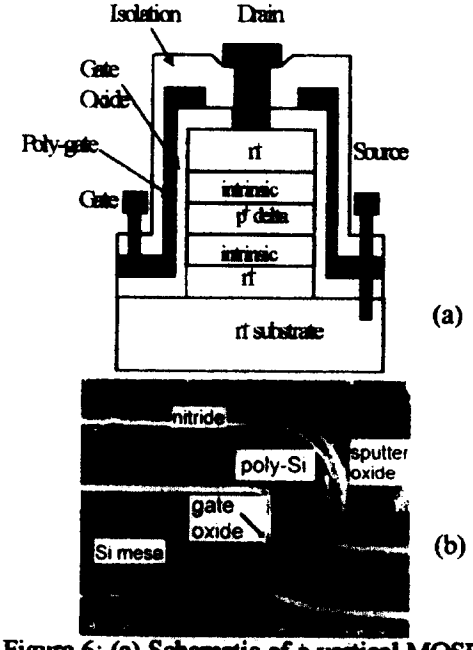

Figure 6: (a) Schematic of a vertical MOSFET with gate oxide surrounding the mesa forming a MOSFET structure. (b) SEM cross-sectional view of the fabricated vertical MOSFET structure.

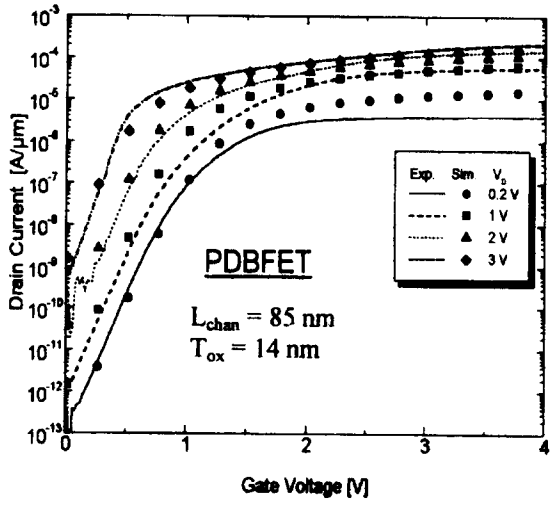

Figure 7: I_d-V_g characteristics for the vertical MOSFET with a channel length of 85 nm by using HIPOX as a gate dielectric.

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