Evaluation of the Impact of Layout on Device and Analog Circuit Performance With Lateral Asymmetric Channel MOSFETs

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***Abstract*—Lateral asymmetric channel (LAC) or single halo devices have been reported to exhibit excellent short channel behavior in the sub-100-nm regime. In this paper, we have quantified the performance degradation in LAC devices due to fingered layouts. Our mixed-mode two-dimensional simulation results show that though the fingered layout of the device limits the performance of these MOSFETs, they still show superior performance over the conventional devices in the sub-100-nm channel length regime. We also present the simulation results of a two-stage operational amplifier with LAC and conventional devices using a 0.13-μm technology with the help of look-up table simulations. Our results show that for the given design specifications, an OPAMP layout with conventional devices occupies 18% more chip area compared to the LAC device.**

***Index Terms*—Analog circuit, channel engineering, lateral asymmetric channel (LAC), look-up table (LUT), MOSFET, quasi-static.**

I. Introduction

THE SHORT-channel behavior of MOS transistors with channel-engineered structures has been extensively studied in the literature [1]–[6]. This includes super steep retrograde (SSR) channel devices, in which the doping profile vertical to the interface is made nonuniform, and halo-doped channel devices, in which the body doping at source and drain ends is made higher compared to the middle of the channel region [1]–[3]. In particular, lateral asymmetric channel (LAC) or single halo (SH) devices, in which a heavily doped channel, also called pocket doping, is present only at the source end but not at the drain end, have been reported recently as most suitable for high-performance analog and mixed-signal circuits in the deep submicrometer regime [7]–[12].

Eliminating the heavily doped region at the drain in usual halo doped devices results in good control over short channel effects such as V_T rolloff, DIBL and channel length modulation and hence in better values of device parameters such as device output resistance and off-currents. This improved performance in SH or LAC devices is observed in comparison to uniform channel devices, SSR devices, and the usual symmetrical halo devices [13], [14]. It has also been reported that the LAC devices have better drive current, transconductance, and cutoff frequencies compared to the above devices [15], [16]. However, with asymmetric devices, there is a restriction in terms of layout since the source and drain are not symmetric. For example, fingered layouts and common centroid layouts cannot be used for these devices in the same way as conventional (symmetric) devices. Because of layout restrictions, the circuit performance would degrade to some extent. This issue needs to be carefully evaluated. This paper, for the first time, addresses this issue and quantifies this degradation using detailed layout and circuit designs. In the existing literature [14], [15], though the circuit performance is quantified with basic analog circuits using two-dimensional (2–D) mixed-mode simulations, these studies have not taken into account the layout constraint, which is the sources of all transistors in a circuit need to be laid out in one direction, existing in asymmetric channel devices.

The motivation for this paper is to address two aspects. First, we quantify the degradation in device analog performance parameters of the devices with fingered layout. The placement of the pocket in the transistor stacked circuit such as cascode amplifier is varied and the performance degradation is quantified with the help of 2-D device and mixed-mode simulations. The corresponding results are reported in Section II. In the second part of this paper, we compare the layout area for a standard two-stage operational amplifier circuit, designed with LAC and conventional technologies. For a realistic comparison between the two technologies, the operational amplifiers were designed for identical specifications. Since compact models are not widely available for LAC devices, large circuits cannot be simulated using standard circuit simulator. All the OPAMP simulations in this paper were performed using a look-up table (LUT) approach, which has been implemented in our group in a general-purpose circuit simulator framework. The accuracy of the LUT simulations is verified with device simulations in Section III. In the same section, layout techniques followed for implementing these circuits, performance degradations and their silicon area requirements are discussed. Finally, Section IV summarizes the important findings of this work.

Manuscript received February 24, 2005. This work was supported by the Department of Science and Technology, Indian Institute of Technology (IIT), Bombay, India. D. V. Kumar and K. Narasimhulu are supported by the Intel Corporation through a fellowship at IIT Bombay. The review of this paper was arranged by Editor R. Singh.

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Digital Object Identifier 10.1109/TED.2005.850941

TABLE I
TECHNOLOGY PARAMETERS AND VOLTAGE SCALING USED FOR DEVICE SIMULATIONS. N_{sc} SHOWS THE CHANNEL DOPING FOR CONVENTIONAL DEVICES, N_{pl} SHOWS THE PEAK POCKET DOPING AT THE SOURCE, AND N_{sl} SHOWS THE DOPING AT THE DRAIN SIDE IN LAC DEVICES

L_G (μm)	0.25	0.18	0.13	0.1	0.07
V_{DD}(V)	2.5	1.8	1.5	1.2	1
V_{DS}(V)	1.25	0.9	0.75	0.6	0.5
T_{ox}(nm)	3	2.5	2	1.5	1.2
V_T (V)	0.35	0.3	0.25	0.2	0.2
X_j (nm)	65	50	40	30	25
N_{sc}(/cm^3)	1.42e17	8.47e17	1.03e18	1.9e18	2.18e18
N_{sl} (/cm^3)	2.03e17	2.12e17	2.4e17	2.43e17	6.14e17
N_{pl}(/cm^3)	2.32e18	2.07e18	1.91e18	1.89e18	2.88e18

II. IMPACT OF LAYOUT ON DEVICE AND CIRCUIT PERFORMANCE

In this section, the details of device/mixed-mode simulations and effect of the position of the pocket on the device and circuit performance are discussed. The doping profiles for both LAC and conventional MOS transistors were generated using a standard ISE DIOS process simulator [22]. The process flow for LAC MOSFETs is identical to that of conventional MOSFETs except for the threshold adjust implant, which was done through a tilted angle implantation from the source side, after the gate electrode formation [8]. The channel implant (BF2) for conventional devices was carried out before the gate oxidation, while for the LAC devices, a tilted channel implant (BF2 at 7°) was done after the gate electrode formation. This implant dose was adjusted to achieve identical threshold voltage for the two devices. The corresponding threshold voltages and channel doping are shown in Table I for all the devices. In this table, N_{sc} represents the channel doping for conventional devices, N_{pl} represents the peak pocket doping at the source end and N_{sl} represents the doping at the drain side in LAC devices. The existing process models were used for both the devices with the device parameters such as junction depth, effective gate length, and deep source/drain depths adjusted to be identical. ISE DESSIS device simulator was used for device simulations with the optimized model parameters tuned with the experimental characteristics using a 0.2-μm fabricated device. Drift-diffusion models were used in device simulations for both the technologies. ISE mixed-mode simulator was used for the circuit simulations [22] except for OPAMP simulations where the mixed-mode simulations become impractical due to large number of transistors. For the ac small signal simulations, a frequency of 1 MHz was used.

Fig. 1(a) shows the simulated device output characteristics for conventional, LAC devices in forward mode (pocket is at the source side) and LAC device in reverse mode (pocket is at the drain side). These simulations were performed at gate over-drive voltages ($V_{GT}s$) of 0.25 and 0.5 V. The device gate length and widths were 0.1 and 1 μm, respectively, while other technology parameters were scaled according to the SIA roadmap as shown in Table I. The threshold voltages for the two devices were adjusted to be of 0.2 V. The improved saturation in the I_D–V_D characteristics for LAC devices in the forward mode operation has been attributed to an improved short-channel performance in these devices [13], [15]. Also, one can notice that the LAC device in the reverse mode operation results in poor current saturation characteristics due to the heavily doped pocket, which appears at the drain end. Higher doping at the drain results in higher drain-induced barrier lowering (DIBL) and hence degraded output resistance. Fig. 1(b) shows transistor analog performance parameters g_m/I_D and small signal drain conductance (g_{ds}) as a function of gate over drive voltage (V_{GT}) for the same devices at a drain voltage of 0.6 V. Better values for these parameters can be seen for LAC devices in the forward mode of operation in the saturation region. Though there is not much degradation in g_m/I_D for reverse LAC devices, there is significant degradation in the drain conductance. This poor reverse source/drain operation would make the LAC devices unsuitable for circuits, which need fingered and common centroid layouts. These layouts are however commonly required for analog/RF circuits to reduce the gate resistance, parasitic capacitance and to improve the matching characteristics of the input differential pair in OPAMP circuits [23]. The impact of layouts on LAC circuit performance issues therefore needs to be systematically investigated, which is the focus of this work.

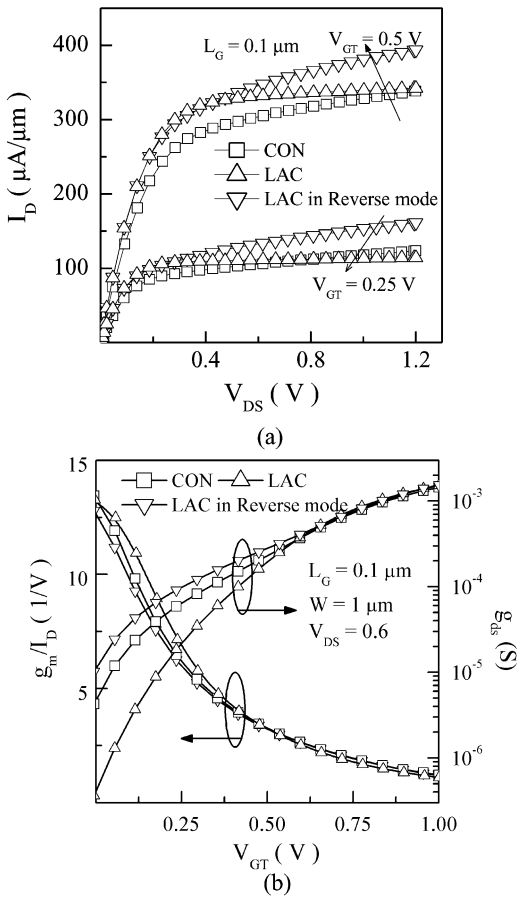

Fig. 1. (a) Simulated output characteristics of conventional, LAC, and LAC in reverse-mode devices at V_{GT} of 0.25 and 0.5 V, $L_G = 0.1$ μm and $W = 1$ μ. (b) Device analog parameters g_m/I_D and drain conductance g_{ds} as function of gate over drive voltage (V_{GT}) at a drain voltage of 0.6 V and gate width is taken as 1 μm.

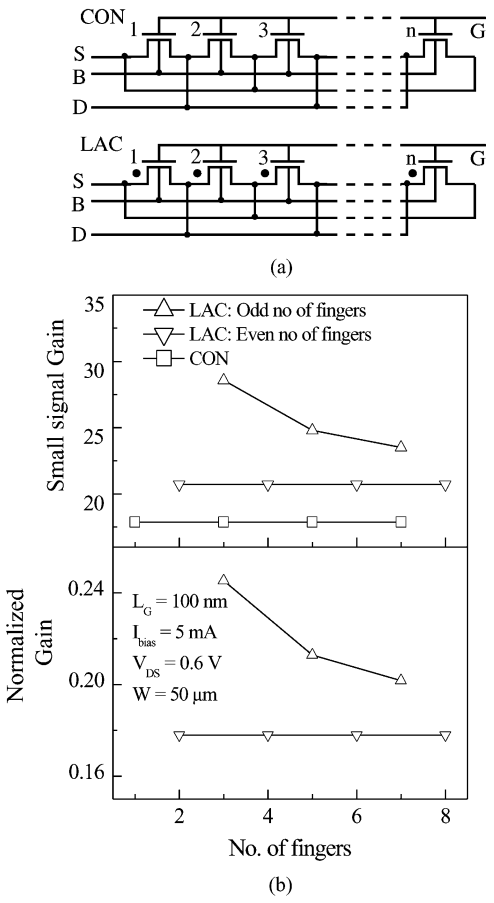

Fig. 2. (a) Fingered device structure used for simulation, black dot indicates the position of the pocket. (b) Small signal gain and the normalized gain as a function of number of fingers for both CON and LAC devices at a biasing current of 5 mA and $L_G = 100$ nm and total device width $= 50\,\mu$m.

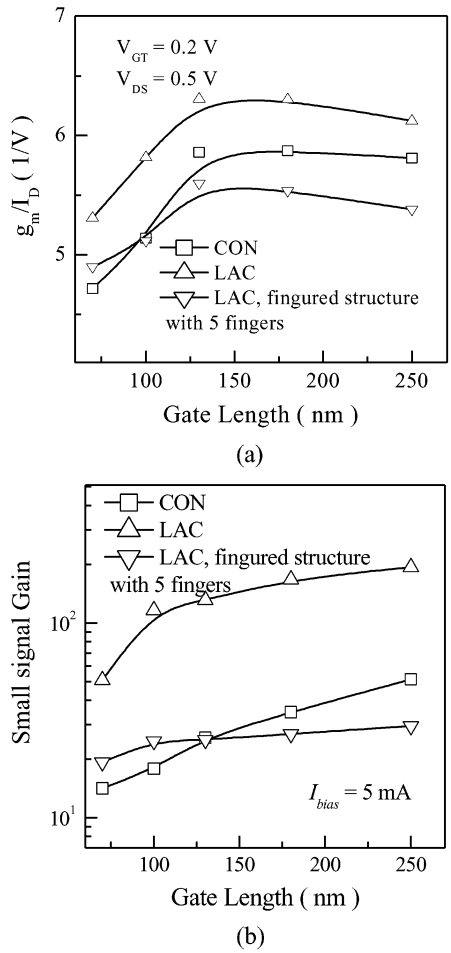

Fig. 3. (a) Device g_m/I_D at a gate over drive of 0.2 V and a drain voltage of 0.5 V. (b) Small-signal gain as a function of channel length for both CON and LAC devices. LAC device withfive fingers is also included. The devices are biased at a constant current of 5 mA and $V_{\rm DS} = V_{\rm DD}/2$, scaled as shown in Table I.

Fig. 2(a) shows the device structures for conventional and LAC devices with *n* number of fingers for simulations, where the black dot indicates the position of the heavily doped pocket in the device. The doping profiles for devices with gate length of 100 nm ($L_{\rm eff} = 75$ nm) were realized using DIOS process simulator. The devices were scaled according to the ITRS roadmap with the technology parameters as given in Table I. Devices with up to eight fingers were simulated and the results were compared with the Conventional devices. Fig. 2(b) shows the simulated device small signal gain and normalized gain as a function of number of fingers at a drain bias current of 5 mA, drain voltage of 0.6 V, and with the transistor dimensions $W = 50\ \mu$m and $L = 100$ nm. The voltage gain of the LAC devices without fingering is 126. As expected, conventional devices show constant gain with increasing number of fingers, while the LAC devices show degraded voltage gain with increasing number of fingers. The reduced output resistance of LAC device in the reverse mode results in the reduction of the overall gain. Also, one can observe that the degradation is constant with even number of fingers while the degradation increases with increasing odd number of fingers. However, it may be noted that at this channel length, the small signal gain of the LAC device is still higher compared to the conventional device. This is due to an overall higher contribution of LAC forward mode devices for this channel length. At this channel length the degradation in the device in reverse mode is not so significant and hence the overall gain is still dominated by the LAC devices in the forward mode. However, it can be seen that the normalized gains with respect to single finger LAC device are drastically reduced both for even and odd fingered devices.

Fig. 3(a) shows the device g_m/I_D at $V_{\rm GT} = 0.2$ V and $V_{\rm DS} = 0.5$ V and Fig. 3(b) shows the small-signal voltage gain at a frequency of 1 MHz as a function of channel length at a constant current bias of 5 mA, drain voltage and other technology parameters as given in Table I. The finger width for all the devices is 10 μm and the number of fingers is equal to 5. One can see that the fingering of the LAC device still retains the advantage of increased small signal gain compared to the conventional devices down to the sub 100 nm regimes. This happens because in the very short channel regimes (below 130 nm), the average doping in the channel region increases with scaling of the LAC devices, as compared to conventional devices. This is true even for LAC reverse mode operation (pocket near the drain), which therefore improves the overall gain with fingering. However, for channel lengths above 130 nm, the gain reduces with fingered structures with the voltage gain falling below that of conventional devices. This is because at these channel lengths, the degradation in the reverse mode LAC is higher due to the increased electric field at

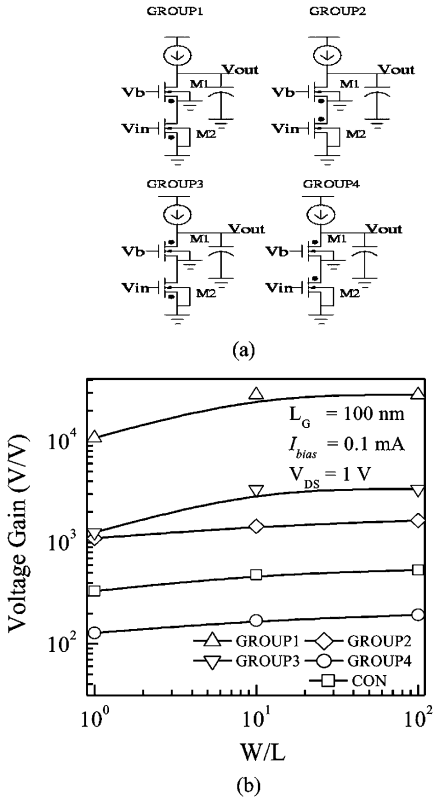

Fig. 4. (a) Circuits used for simulations, where the black dot indicates the position of the pocket in the device. (b) Circuit voltage gain as a function of transistor W/L at $I_{\rm bias} = 0.1$ mA with the dc voltage at the output node equal to 1 V.

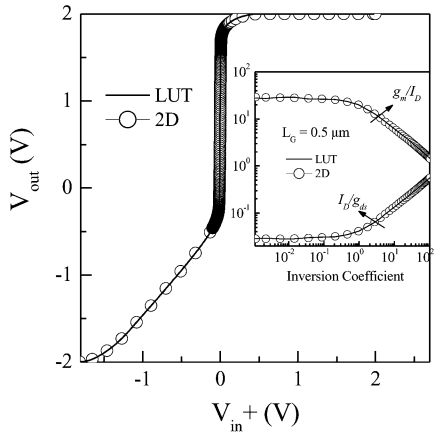

Fig. 5. DC transfer characteristics of the differential amplifier with 2-D and LUT simulations. In the inset, g_m/I_D and $I_D/g_{\rm ds}$ are shown as a function of inversion coefficient at $V_{\rm DS} = 1$ V and $V_{\rm SB} = 0$, with $L_G = 0.5$ μm.

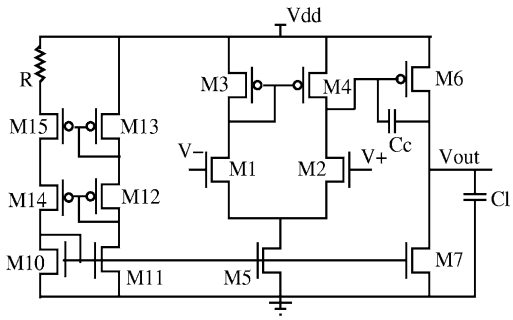

Fig. 6. Circuit schematic of the OPAMP used for simulations, with the transistor sizes as shown in Table III. For the designed specifications, R = 2 K, and C_c = pf.

the drain junction, which affects the short channel performance. Fig. 4(b) shows the voltage gain of the cascode amplifier as a function of transistor *W/L* of the driver transistor biased at a current of 0.1 mA and a dc output bias of 1 V and with a capacitive load of 100 fF. $V_{\rm b}$ was adjusted to get the specified bias current at this dc output voltage. Though this voltage was forced to be 1 V for the simulations, in practice common mode feedback circuits will maintain this voltage to a constant value. The ac small signal simulations were done at a frequency of 1 MHz and voltage gain of the circuit has been plotted for all the circuit configurations shown in the Fig. 4(a). Simulations were also done using the conventional devices for comparison purposes. The transistor channel length is taken as 0.1 μm for all the simulations. The group 4 combination results in an overall circuit voltage gain less than the conventional counter part at all the gate widths. This result also shows that considerable improvement in the overall voltage gain can be obtained even when one of the pockets is present at the drain side. However, the group 1 combination gives the highest improvement for LAC devices, where the pocket for both the driver and biasing devices is present near the source side.

III. Two-Stage OPAMP Area Requirements

The two-stage OPAMP circuit is simulated using the LUT approach, which is implemented in a public-domain general-purpose circuit simulator Sequel [17]. In this section, we first verify the accuracy of LUT approach with the help of device and mixed-mode circuit simulation. A set of dc currents and charges generated using device simulations/measurements can be used as look-up-tables for the LUT simulations. A suitable interpolation scheme is then employed to obtain the values of currents and charges at any arbitrary biasing point [24]. No approximations are made in extracting the terminal charges and currents of the MOS device. The interpolation scheme used in this paper is based on the approach enumerated by Meijer *et al.* [18]. Exponential functions are used to model the I_D-V_G in the subthreshold region, while polynomial functions of degree 3 are used elsewhere as the primary one-dimensional basis functions [18]. For generating the LUTs, we have used the Dessis device simulator and the extraction procedure for generating the terminal currents and charges is described in [21] and [25]. The accuracy of the LUT approach is critically examined for analog circuit simulations, using a detailed comparison of LUT simulations with 2-D mixed-mode circuit simulations.

Fig. 5 shows the transfer characteristics of the basic single-ended differential amplifier circuit simulated using ISE mixed-mode and LUT simulators. The circuit is simulated in 0.13-μm technology. One can clearly observe the accuracy of the interpolation scheme and the LUT approach implemented in this paper. In the inset of Fig. 5, accuracy of the LUT approach on device analog parameters g_m/I_D and $I_D/g_{\rm ds}$ has been shown as a function of normalized I_D (termed as inversion coefficient), where the normalization is done according to the method presented in [26]. We have also checked the validity of LUT approach as a function of frequency and till nearly 0.6 times f_T, the prediction of g_m is well within 2% error, and the error in predicting $C_{\rm dg}$ is therefore much less.

TABLE II
TABLE SHOWING THE OPAMP DESIRED SPECIFICATIONS AND THE ACHIEVED PERFORMANCE PARAMETERS WITH LUT SIMULATIONS FOR BOTH CON AND LAC TECHNOLOGIES

Parameter	Desired	LAC	CON
Bias Current (μA)	100	100	100
Unity Gain Freq.(MHz)	20	20.66	20.58
Phase Margin (Deg)	50	49.2	48
Slew Rate (V/μsec)	40	35.7	35.7
Gain (dB)	82.3	82.16	82.38

TABLE III
THE TRANSISTOR SIZES OF OPAMP DESIGNED FOR THE SPECIFICATIONS IN TABLE II FOR BOTH CON AND LAC TECHNOLOGIES

Transistor	LAC	CON
$(W/L)_1 = (W/L)_2$	2.0/0.5	3.0/0.5
$(W/L)_3 = (W/L)_4$	5.0/0.7	4.0/0.7
$(W/L)_5$	4.0/0.5	5.0/0.5
$(W/L)_6$	80/0.7	98/0.9
$(W/L)_7$	32/0.5	86/0.9
$(W/L)_{10} = (W/L)_{11}$	4.0/0.5	5.0/0.5
$(W/L)_{12} = (W/L)_{13} = (W/L)_{14}$	33/0.7	35/0.7
$(W/L)_{15}$	133/0.7	141/0.7

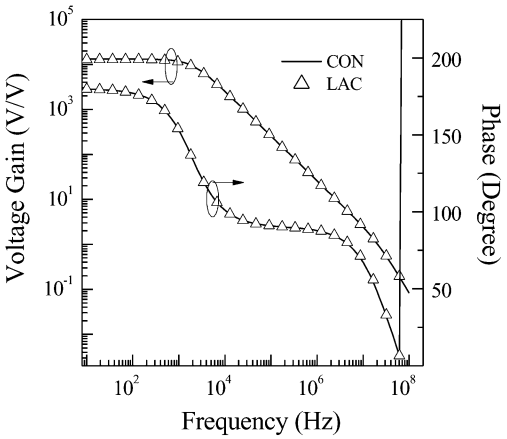

Fig. 7. Frequency response of the operational amplifier simulated using LUT approach. The circuits in CON and LAC technologies are simulated in a 0.13-μm technology for the specifications given in Table II.

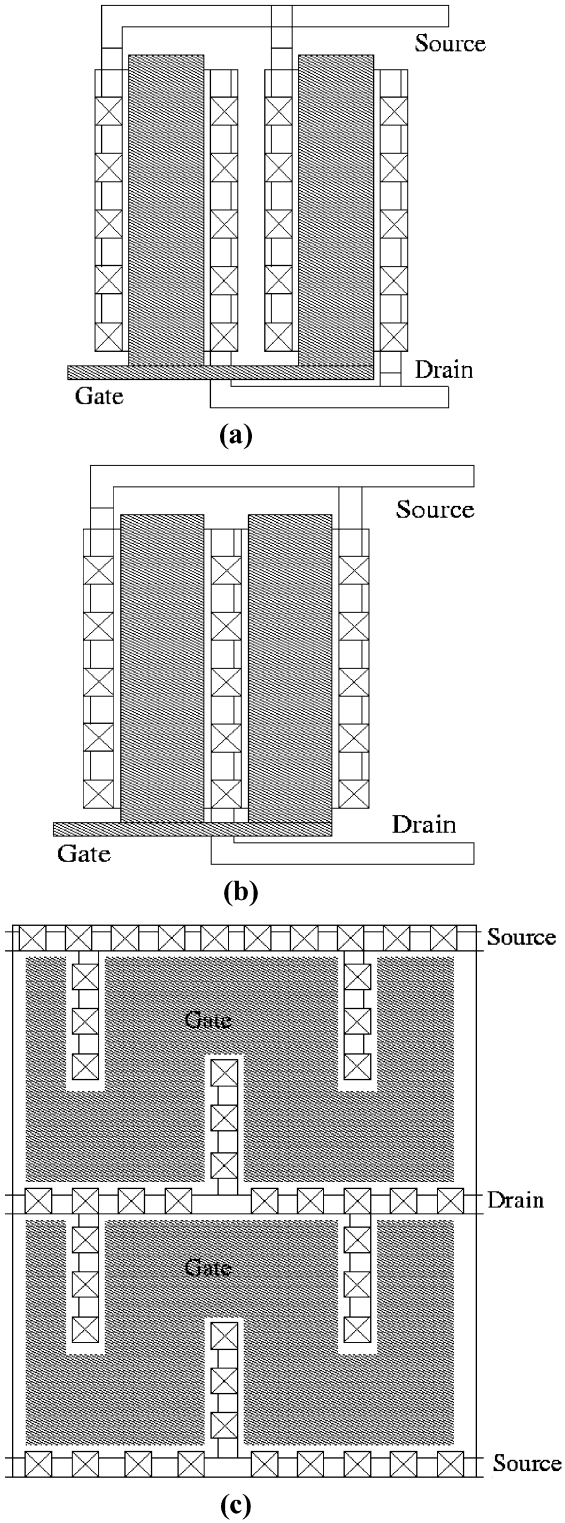

Fig. 8. (a) Transistor layout schematic (fingered layout but source and drains are not shared) used for LAC technologies. (b) Layout schematic of fingered structure with source/drains shared. (c) Serpentine layout schematic. For CON technologies, (b) and (c) layouts are used.

In this section, the results of a two-stage OPAMP shown in Fig. 6 with a capacitive load of 10 pf, simulated in 0.13-μm technology using LUT approach have been presented for both conventional and LAC technologies. OPAMPS in both the technologies were designed for identical specifications and the area required for both the technologies was estimated using Magic-7.1 layout editor. The desired specifications of the OPAMP and the actual values of specifications achieved with LUT simulations for both the technologies are shown in Table II and the designed transistor sizes for both the circuits are shown in Table III. A standard analog circuit design procedure was followed for designing the OPAMP circuit, as given in [27]. One can notice that the minimum transistor channel length used for this circuit was kept 0.5 μm to achieve the adequate output resistance, larger voltage gains and improved matching characteristics. As a common practice, in analog design, minimum

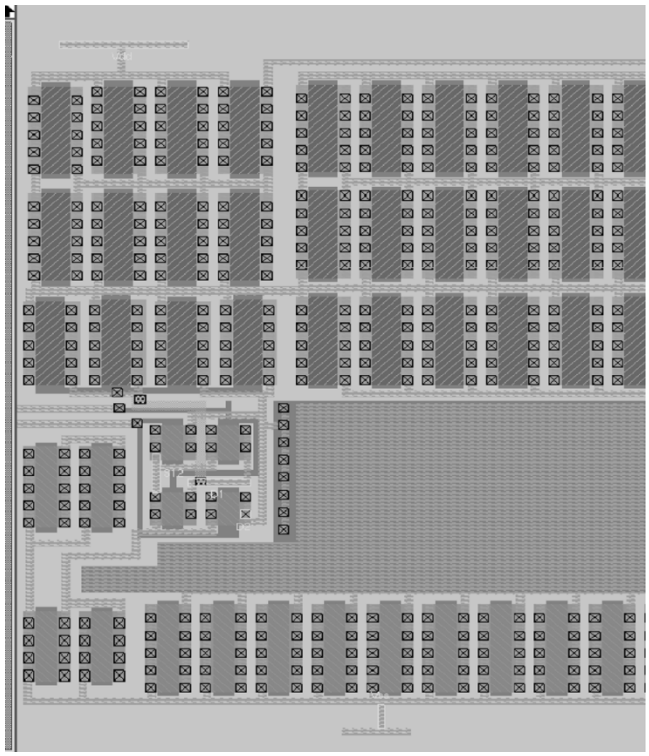

Fig. 9. Schematic of the layout of the complete OPAMP circuit realized in LAC technologies.

channel length is kept four times to that of minimum feature size in the existing technology. Due to the improved short channel performance of LAC device, smaller area LAC devices can be used for the given circuit specifications, reducing the overall parasitic capacitances in the circuit, however, due to large compensation capacitance, this influence of the reduced parasitic capacitance is not seen. The frequency response of the OPAMP for LAC and conventional technologies is shown in Fig. 7. One can see that the OPAMP are designed for nearly identical specifications for both the technologies.

Fig. 8 shows the transistor layouts used for calculating the area requirement for both the technologies. Fig. 8(a) is the layout (fingered layout but source and drains are not shared) used for LAC technologies, due to the constraint of placing all sources on one side and this configuration is used for the estimation of the area requirement. Fig. 8(b) and (c) shows two other layout schemes (one sharing the source/drain and the other a serpentine layout) used for conventional technologies. Serpentine layout is the most compact version for conventional technologies, making this comparison to be the worst case. Fig. 9 shows the layout of an OPAMP circuit using LAC technology, considering the layout constraints. We have laid out the OPAMP for conventional devices with two layout techniques discussed in Fig. 8(b) and (c) and the area required is estimated for all the different cases. It can be seen that despite the layout constraints, LAC circuit results in a reduction in the overall area, for the given circuit specifications, when compared to CON technologies. This is due to the superior performance of LAC devices enabling the use of smaller gate area transistors. We have seen an improvement of 37% and 18% gain in circuit area for LAC technologies over conventional technologies when fingered layouts with source/drain sharing and serpentine schemes are used for conventional devices. This makes the LAC device suitable for analog applications, despite the constraints imposed by the asymmetric nature of the device.

IV. Conclusion

The effects of layout constraint on the device and circuit performance were quantified for lateral asymmetric channel devices and the results were compared with conventional devices. Though LAC devices are reported to outperform conventional and SSR devices for analog applications, it is believed that fingered layouts could degrade the over all performance in LAC designs. However, as our results show, LAC devices, despite the layout constraints, still exhibit superior performance compared to conventional devices. Our results on two-stage OPAMP circuit show that significant improvement in the silicon area can be achieved with LAC technologies, even after considering the layout constraint, making these technologies suitable for high performance RF analog applications.

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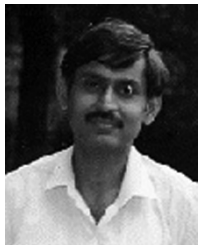

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