

$1/f$ Noise in Drain and Gate Current of MOSFETs With High- k Gate Stacks

P. Magnone, F. Crupi, G. Giusi, C. Pace, E. Simoen, C. Claeys, *Fellow, IEEE*, L. Pantisano, D. Maji, V. Ramgopal Rao, *Senior Member, IEEE*, and P. Srinivasan

(Invited Paper)

Abstract—In this paper, we investigate the quality of MOSFET gate stacks where high- k materials are implemented as gate dielectrics. We evaluate both drain- and gate-current noises in order to obtain information about the defect content of the gate stack. We analyze how the overall quality of the gate stack depends on the kind of high- k material, on the interfacial layer thickness, on the kind of gate electrode material, on the strain engineering, and on the substrate type. This comprehensive study allows us to understand which issues need to be addressed in order to achieve improved quality of the gate stack from a $1/f$ noise point of view.

Index Terms—Drain noise, gate noise, high- k dielectric, MOSFET, $1/f$ noise.

I. INTRODUCTION

THE RELENTLESS push for more and faster devices on a chip in CMOS technology is driving the demand for shrinking geometries. The accompanying gate dielectric thickness decrease leads to a large gate-current leakage due to quantum mechanical tunneling of carriers through the thin gate oxide [1], [2] and, therefore, to higher static power dissipation. That problem is alleviated in novel gate stacks by introducing high- k materials in order to achieve the same gate dielectric capacitance of conventional SiO₂ with a thicker dielectric layer. It should be noted that, for decades, the quality of the silicon/silicon dioxide interface was a strong point of the silicon technology and a lot of effort has been put in order to replace the silicon dioxide with high- k dielectrics. Difficulties arise in order to address typical issues like threshold voltage shift, mobility reduction, bias temperature instability, and stress-induced leakage current, which are common in high- k materials [3], [4]. On the other hand, several studies have shown that low-

frequency drain-current noise measurements represent one of the most powerful tools to investigate the material defectiveness [5]–[14]; therefore, noise analysis is very useful to validate the quality of the gate stack when new materials are introduced. Furthermore, a new model has been recently proposed in [15], where it is shown that low-frequency gate-current $1/f$ noise can also be used as a source of information for assessing the quality of the gate stack in MOS structures. This investigation technique is very suitable in the case of large gate-current leakage, where the accuracy of most traditional techniques (combination of high-frequency and quasi-static C - V [16], charge pumping [17], [18], and drain noise measurements) could be corrupted. The idea behind this model [15] is that the charging/discharging of defects in the dielectric can block/unblock effective portions of the gate area, thus causing a fluctuation in the gate current. With this in mind, the gate noise is proportional to the total amount of traps that can be charged/discharged in the dielectric.

In this paper, both drain- and gate-current noise measurements are used to check the quality of high- k gate stacks in MOSFETs. In order to better localize the sources of gate-stack quality degradation, the impact on noise of several parameters is exploited: high- k material, interfacial layer (IL) thickness, gate electrode material, strain engineering and substrate material.

The remainder of this paper is organized as follows. In Section II, the details about the typical high- k dielectrics investigated and about the measurement system are given. In Section III, the methodology utilized for data elaboration and interpretation is described. In Section IV, the experimental results are shown, and in Section V, the main conclusions are summarized.

II. EXPERIMENTAL

In this paper, we examined Hf-based dielectrics as replacement materials of conventional SiO₂ or SiON. In particular, two types of high- k dielectrics were used in the gate stacks investigated: HfO₂ or HfSiON with different percentage of hafnium. These materials were deposited by means of atomic layer deposition (ALD) or metallo-organic chemical vapor deposition (MOCVD) [2]. Furthermore, a SiO₂ or SiON stratum was comprised between the substrate and the high- k dielectric as an IL.

Noise measurements were done on MOSFETs by means of a specially designed instrumentation setup [19]. Drain-current noise measurements were carried out in linear region with

Manuscript received October 8, 2008; revised March 12, 2009. First published April 7, 2009; current version published June 5, 2009.

P. Magnone, F. Crupi, G. Giusi, and C. Pace are with the Dipartimento di Elettronica, Informatica e Sistemistica, University of Calabria, 87036 Cosenza, Italy (e-mail: magnonep@deis.unical.it).

E. Simoen and L. Pantisano are with the Interuniversity Micro-Electronics Center, 3001 Leuven, Belgium.

C. Claeys is with the Interuniversity Micro-Electronics Center, 3001 Leuven, Belgium, and also with the Department of Electrical Engineering, KU Leuven, 3001 Leuven, Belgium.

D. Maji and V. R. Rao are with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400 076, India.

P. Srinivasan is with Texas Instruments Incorporated, Dallas, TX 75243 USA.

Digital Object Identifier 10.1109/TDMR.2009.2020406

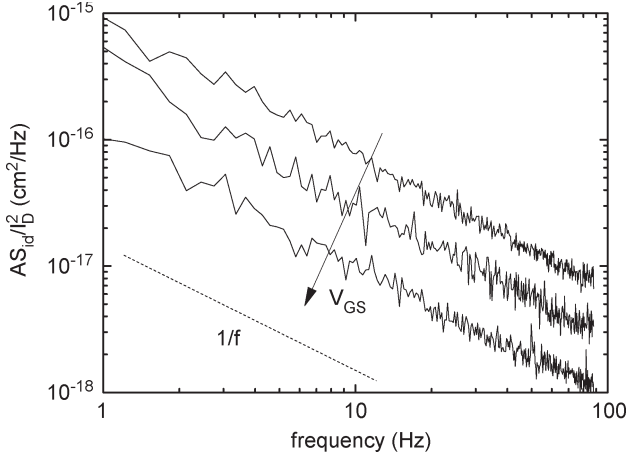


Fig. 1. Drain-current noise spectra normalized with respect to the device area and the dc drain-current square. Typical $1/f$ spectra are observed for different V_{GS} values.

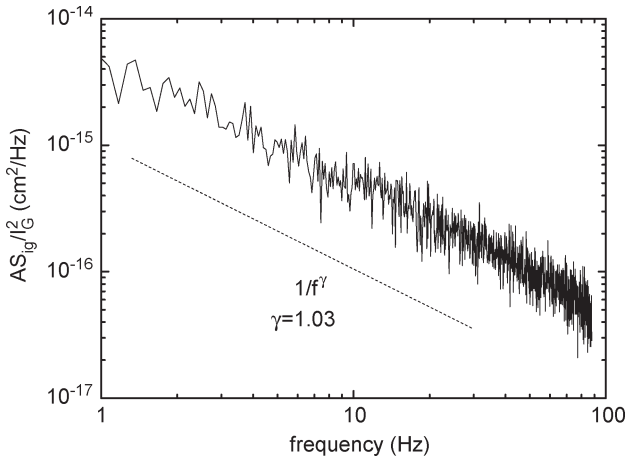


Fig. 2. Gate-current noise spectrum normalized with respect to the device area and the dc gate-current square. By fitting the spectrum with a $1/f^\gamma$ law, the coefficient γ is found to be very close to one ($\gamma = 1.03$).

the drain-to-source voltage $V_{DS} \leq 50$ mV, while for the gate-current noise measurements, $V_{DS} = 0$ V was applied. Static characterization was performed with a 4200-SCS Keithley parameter analyzer in order to measure I_D - V_{GS} and I_G - V_{GS} curves and then to extract typical parameters such as transconductance g_m and threshold voltage V_T .

III. DATA ANALYSIS METHODOLOGY

In this paper, the spectra were measured for both drain- and gate-current noises. The typically observed spectra are shown in Figs. 1 and 2 for the drain and gate currents, respectively. In both cases, a $1/f$ -like noise is found. The obtained power spectral densities are then fitted with a law $1/f^\gamma$ in a frequency range of 1 decade, and the coefficients γ 's are extracted. It can be easily checked that in Figs. 1 and 2, γ is close to one. Moreover, the dc drain and gate currents are measured at the same time.

All the data reported in this paper are extracted in samples exhibiting $1/f$ noise. In the following, we will show how these measurements are treated, in order to obtain a figure of merit for the MOSFETs investigated.

A. Drain Current

The drain-current power spectral density S_{id} normalized with respect to the square of the dc drain current I_D and with respect to the channel area $A = WL$ is measured in the frequency range of 1–100 Hz and evaluated at a fixed frequency ($f = 25$ Hz) as a function of the gate voltage overdrive. In order to understand which mechanism dominates the drain flicker noise, a common method consists in checking the normalized S_{id} dependence on the gate voltage overdrive ($V_{OV} = V_{GS} - V_T$) with the MOSFET biased in the linear region. When $A \cdot S_{id}/I_D^2 \propto (1/N)^2 \propto 1/(V_{GS} - V_T)^2$, where N is the number of electrons in the channel, the noise is attributed to the fluctuation of charge carriers which are trapped and detrapped by oxide traps [7], [20], [21]. Otherwise, if $A \cdot S_{id}/I_D^2 \propto 1/N \propto 1/(V_{GS} - V_T)$, the noise is attributed to the fluctuation of the mobility in the inversion layer [5]. Moreover, correlated carrier number/mobility fluctuation is also possible in the middle case [6], [21]. Based on the dominant source of noise, a different figure of merit can be computed.

If carrier number fluctuation dominates, then the trap density in the dielectric per unit energy and unit volume can be extracted as [7]

$$N_t = \frac{S_{id} C_{EOT}^2 W L f (V_{GS} - V_T)^2 \gamma}{q^2 k T I_D^2} \quad (1)$$

where q is the elementary electron charge, kT is the thermal energy, γ is the attenuation coefficient [7], and C_{EOT} is the gate dielectric capacitance per unit area. Conversely, from the study in [6], the g_m dependence on the gate voltage overdrive [14] is taken into account. In (1), the trap density is supposed to be uniform in energy and in space. Moreover, the traps are considered to be situated close to the channel interface. These assumptions are not verified in the case of multistack gates. Therefore, in this case, the trap density should be read as an effective number.

If mobility fluctuation dominates, then the so-called Hooge parameter can be extracted as [11]

$$\alpha_H = \frac{W L S_{id} f C_{EOT} (V_{GS} - V_T)}{I_D^2 q} \quad (2)$$

B. Gate Current

The gate-current power spectral density S_{ig} is measured in the frequency range of 1–100 Hz, and taken at a fixed frequency ($f = 1$ Hz) and in accordance with the study in [15], a figure of merit for the quality of the gate stack can be extracted as

$$GNP \equiv \frac{S_{ig} f A}{I_G^2} \quad (3)$$

where I_G is the dc gate current and GNP is defined as the gate noise parameter. The extracted value is independent on the gate area and on the bias point in the case of a uniform energy distribution of traps. It is worth noting that the frequency value chosen does not influence the GNP since this analysis applies for $1/f$ noise spectra.

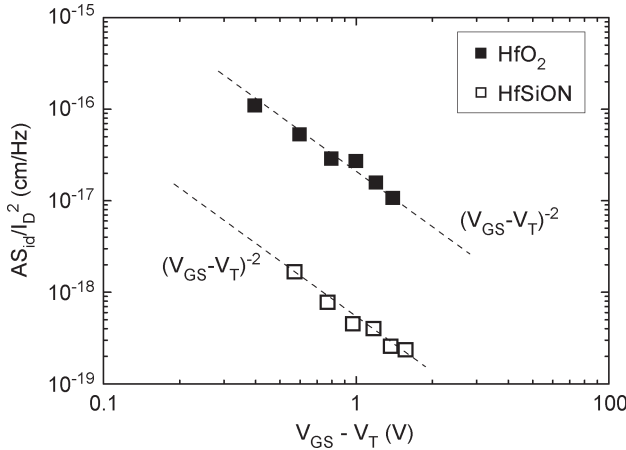


Fig. 3. Normalized drain-current spectral density at $f = 25$ Hz as a function of the gate voltage overdrive for different high- k dielectrics. In the measured devices, the channel width was $10 \mu\text{m}$, while the channel length ranged from 0.18 to $0.25 \mu\text{m}$. N-MOSFETs with HfO_2 dielectric show 1 decade higher noise than the ones with HfSiON .

Note that the expression of the GNP is similar to the Hooge parameter, generically defined as

$$\alpha_H \equiv \frac{S_i f N}{I^2} \quad (4)$$

where N is the total number of charge carriers and I is the dc current. As discussed previously, the Hooge parameter is widely used in the case of the drain noise measurements, where N is proportional to the gate area A . Thus, the only difference between the two definitions is that the Hooge parameter contains an additional factor corresponding to the number of charge carriers per unit area. The reason why the GNP is not normalized for this factor is that experimental data show that the GNP is quite independent on the bias point and thus on the number of charge carriers per unit area [15].

The GNP has a twofold meaning. On one hand, it can be considered as an empirical parameter for the measurement of the normalized gate noise. On the other hand, it can be related to physical quantities of the gate stack on the basis of the model proposed in [15]. In the last case, the GNP is proportional to the trap density in the dielectric.

IV. EXPERIMENTAL RESULTS

A. Impact of High- k Material

N-channel MOSFETs with two different gate stacks were compared: a double layer consisting of a 4.5-nm HfO_2 film on the top of a 1-nm SiO_2 IL with an EOT (equivalent oxide thickness) of 1.7 nm and a double layer formed by a 2-nm $\text{Hf}_x\text{Si}_{1-x}\text{ON}$ ($x=0.23$) film on the top of a 1-nm SiON IL with an EOT of 1.6 nm . Both devices were polysilicon gated [14].

From the drain point of view, two main observations can be made based on the results in Fig. 3. First, the normalized drain-current noise magnitude for the HfO_2 gate stack is significantly higher with respect to the HfSiON one, thus indicating a worsening of noise behavior when the Hf content is increased. Second, it is clear that in both gate stacks, the $1/f$ noise dominating

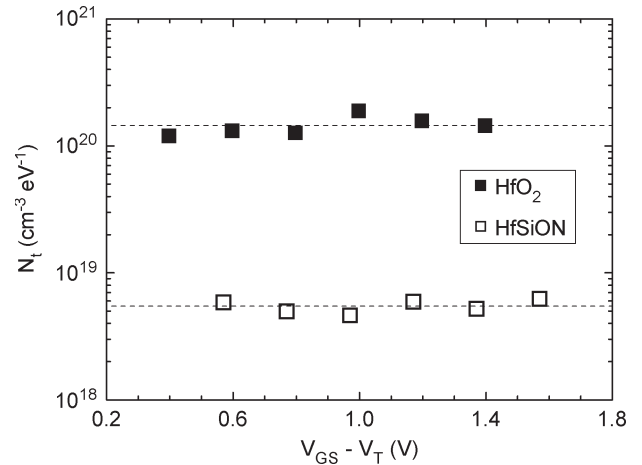


Fig. 4. Trap density per unit volume and unit energy as a function of the gate voltage overdrive. The channel width was $10 \mu\text{m}$, while the channel length ranged from 0.18 to $0.25 \mu\text{m}$. Lower defect density can be observed in the case of HfSiON dielectric because of the lower hafnium content with respect to the HfO_2 dielectric.

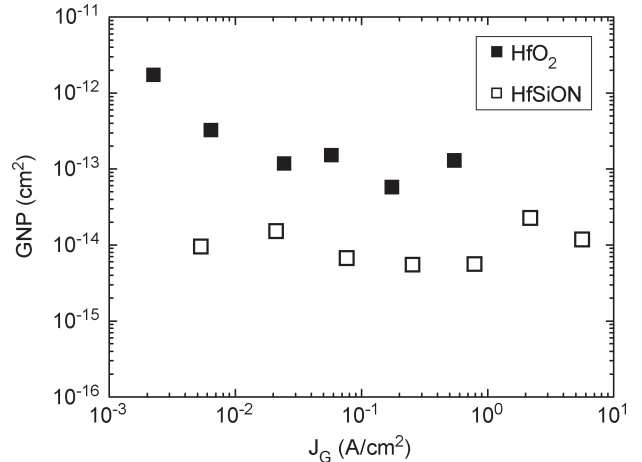


Fig. 5. GNP as a function of the gate-current density for HfO_2 - and HfSiON -based dielectrics. The channel width was $10 \mu\text{m}$, while the channel length ranged from 0.18 to $0.25 \mu\text{m}$. The observed GNP values indicate an improved quality of the gate stack for the HfSiON samples.

mechanism is carrier number fluctuation since $A \cdot S_{id}/I_D^2 \propto 1/(V_{GS} - V_T)^2$. Under this supposition, the trap density N_t can be extracted by using (1), and the results are shown in Fig. 4. The defect density in the HfO_2 layer ($10^{20} \text{ cm}^{-3} \cdot \text{eV}^{-1}$) is more than one decade higher with respect to the case of HfSiON gate stacks ($5 \times 10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$). Typical trap density extracted for a MOSFET with a conventional SiON dielectric and similar EOT is comprised in the range of 10^{17} – $10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ [22], [23]. Therefore, an increase of defectivity in the gate dielectric is observed in both high- k materials with respect to conventional SiON .

The GNP values extracted from gate noise measurements are shown in Fig. 5. HfO_2 samples exhibit GNP values one decade larger with respect to the HfSiON ones. These results confirm what we observed for the drain noise data, i.e., a large trap density in the hafnium dioxide with respect to the hafnium silicate. In [15] and [24], it is shown that a typical value of GNP for a standard SiON gate dielectric is around 10^{-16} cm^2 . That

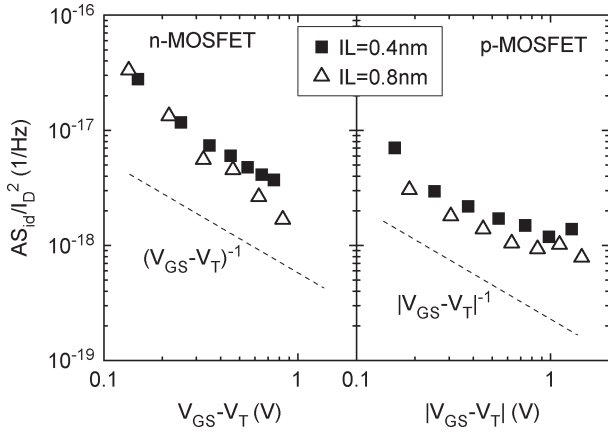


Fig. 6. Normalized drain-current spectral density at $f = 25$ Hz as a function of the gate voltage overdrive for n-MOSFETs and p-MOSFETs having different IL thicknesses. All the MOSFETs under investigation had $W = 10 \mu\text{m}$ and $L = 1 \mu\text{m}$. A slight increase of noise is observed reducing the IL thickness.

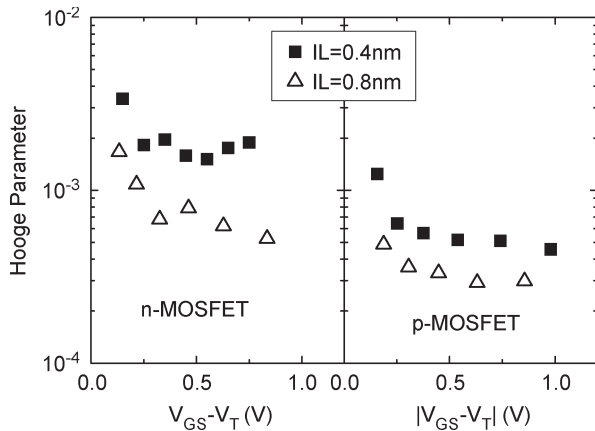


Fig. 7. Hooge parameter values extracted for n-MOSFETs and p-MOSFETs with different IL thicknesses. The MOSFETs had $W = 10 \mu\text{m}$ and $L = 1 \mu\text{m}$. In both types of MOSFETs, the Hooge parameter increases when the IL decreases.

value is three orders of magnitude lower with respect to the HfO_2 dielectric, while an intermediate value is observed for the hafnium silicate devices.

B. Impact of IL

The low-frequency drain-current noise properties were investigated in n- and p-MOSFETs with two different SiO_2 IL thicknesses: 0.4 and 0.8 nm. In both cases, HfO_2 was deposited as high- k dielectric. For p-MOSFETs, the overall EOT's obtained were 1.31 nm in the case of $IL = 0.4$ nm and 1.35 nm for $IL = 0.8$ nm, while for n-MOSFETs, EOT's were 0.92 nm for $IL = 0.4$ nm and 1.44 nm for $IL = 0.8$ nm. PVD TiN/TaN was employed as metal gate [25]. Fig. 6 shows the normalized drain-current noise spectral density dependence on the gate voltage overdrive. For n-MOSFETs, the normalized S_{id} varies as $(V_{GS} - V_T)^{-1.5}$ for the 0.8-nm IL thickness, which highlights that noise is due to correlated number-mobility fluctuations, and $(V_{GS} - V_T)^{-1}$ for 0.4 nm, which points out that noise is mainly due to mobility fluctuation. For p-MOSFETs, the noise mechanism points to Hooge's mobility model. For both types of MOSFETs, a small increase of noise is observed for reduced

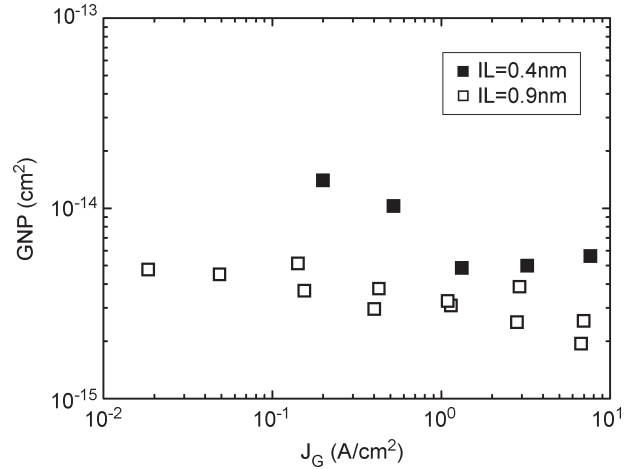


Fig. 8. GNP as a function of the gate-current density in n-MOSFETs with different IL thicknesses. In both cases, the channel width was $10 \mu\text{m}$, and the channel length was $1 \mu\text{m}$. The higher GNP for $IL = 0.4$ nm points to a degradation of the quality of the gate stack with respect to $IL = 0.9$ nm.

IL thickness. Nevertheless, if we look at the extracted Hooge's parameter in Fig. 7, the dependence on the IL thickness is more evident.

The gate-current noise measurements were performed on n-MOSFETs having the following gate stacks: 0.4 nm of SiON as interfacial layer, HfO_2 as gate dielectric, and TiN/TaN as gate electrode ($EOT = 0.9$ nm); 0.9 nm of SiON as interfacial layer, HfO_2 as gate dielectric, and TiN as gate electrode ($EOT = 1.4$ nm). The extracted GNP values are shown in Fig. 8. In accordance with the drain noise measurements, an increase of GNP is observed for a thinner interfacial layer thickness. These experimental observations suggest that bringing the high- k layer closer to the Si-SiO₂ interface enhances the $1/f$ noise in both gate and drain currents. Moreover, the enhanced $1/f$ drain noise due to mobility fluctuations is consistent with the lower mobility values observed in high- k gate stacks with lower IL thickness [26], [27].

C. Impact of Gate Electrode

In order to understand the impact on noise of the interface between high- k dielectric and gate electrode in MOSFET devices, a submonolayer of HfO_2 was sandwiched between conventional SiON dielectric and polysilicon gate. N-MOSFETs and p-MOSFETs were fabricated with a conventional SiON dielectric. Before the polysilicon deposition as a gate, in some samples, a thin HfO_2 layer was deposited by means of ALD, resulting in a partially closed film roughly 0.3 nm thick. The overall EOT was around 1.6 nm for both n-MOSFETs and p-MOSFETs [24].

In Fig. 9, the normalized drain-current noise is shown for both n-MOSFETs and p-MOSFETs. In the case of n-MOSFETs, the first observation that we can do is that at low gate voltage overdrive, the noise mechanism is dictated by carrier number fluctuation, while at high gate voltage, other effects become dominant like correlated carrier-mobility fluctuation or noise coming from the series resistance [28], [29]. Second, an increase of noise is observed in the regime of number

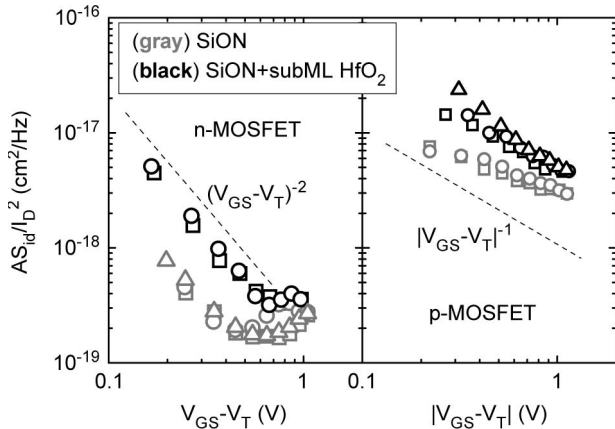


Fig. 9. Normalized drain-current spectral density at $f = 25$ Hz as a function of the gate voltage overdrive in $10\text{-}\mu\text{m}$ -wide and $1\text{-}\mu\text{m}$ -long MOSFETs. A submonolayer of HfO_2 is able to increase the noise in both n-MOSFETs and p-MOSFETs.

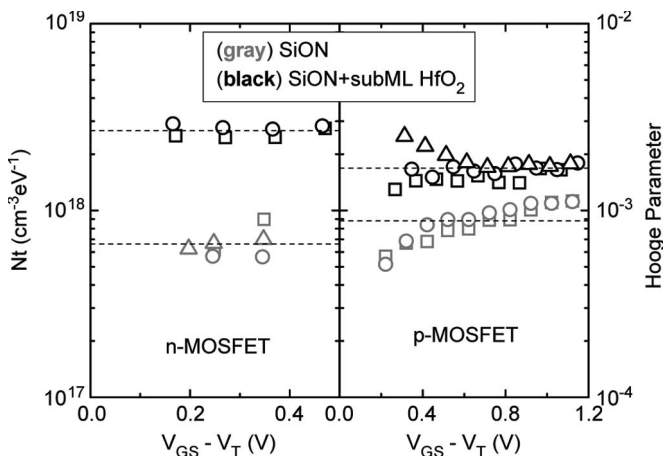


Fig. 10. Trap density and Hooge parameter extracted for n-MOSFETs and p-MOSFETs, respectively. Both figures of merit point to a large amount of defects at the interface between HfO_2 and polysilicon.

fluctuation in the case of HfO_2 submonolayer because of the high defect density close to the polysilicon gate. In Fig. 10, the trap density is extracted in the regime of number fluctuation, and an increase of $2 \times 10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ is observed in the samples with a submonolayer of HfO_2 . It is worth noting that in these samples, the trap density value is just an effective value since the model behind (1) is based on the hypothesis that the defects are close to the silicon interface. For p-MOSFETs, the dominant noise mechanism in Fig. 9 seems to be mobility fluctuations in the whole range of bias conditions as usually observed in the case of p-MOSFETs [30], [31]. As suggested in [32], the different dominant noise mechanism in the case of p-MOSFETs with respect to n-MOSFETs can be explained because of the lower carrier mobility in the channel. Since the mobility fluctuation mechanism dominates in p-MOSFETs, it is expected that the remote phonon scattering due to the HfO_2 submonolayer [33]–[36] should affect the drain-current noise. Nevertheless, that impact is much lower with respect to the case of n-MOSFETs. This is because the noise increase caused by the remote phonon scattering due to the HfO_2 submonolayer is partially hidden by the high noise level due to the mobility

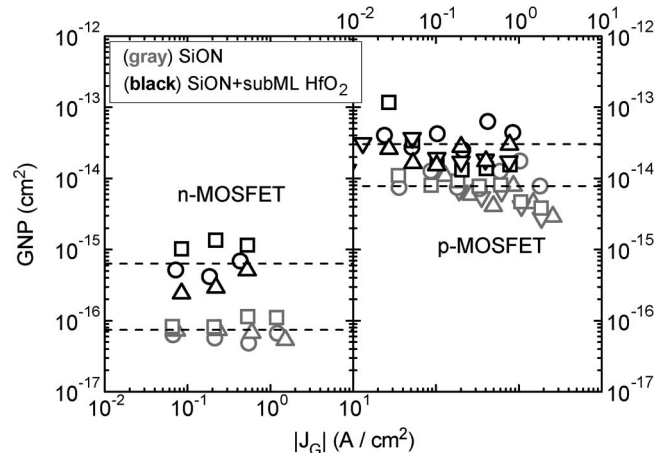


Fig. 11. GNP as a function of the gate-current density for n-MOSFETs and p-MOSFETs. In both cases, the channel width was $10 \mu\text{m}$, and the channel length was $1 \mu\text{m}$. The increase of noise due to the presence of HfO_2 is more enhanced with respect to the one observed in Fig. 9. This is because the GNP is more sensitive to the traps close to the upper interface.

fluctuations coming from the lattice scattering. In Fig. 10, one can see that the presence of HfO_2 at the interface with the polysilicon doubles the value of the Hooge parameter.

In Fig. 11, we can observe that the GNP for n-MOSFETs and p-MOSFETs increases with the presence of the submonolayer of HfO_2 . Note that the relative increase in GNP is around 4 and 10 for p-MOSFET and n-MOSFET, respectively. The impact of the defects due to the HfO_2 submonolayer is more evident in the case of gate-current noise than in the case of drain-current noise. This is because the traps far from the channel interface have a limited effect on the drain current, while the gate current is more sensitive to the traps close to the gate side, since they locally influence the potential barrier profile and then the carrier tunneling. Moreover, it is worth noting that noise levels are higher in p-MOSFETs, even in the reference devices. This result is in agreement with the study of Morfouli *et al.* [22]. They reported that in the case of SiON dielectric, p-MOSFETs show a larger trap density with respect to the n-MOSFETs. This can explain why p-MOSFETs have higher noise than n-MOSFETs.

Furthermore, in order to evaluate the impact of the kind of gate electrode, we can compare the previous experiments reported in Sections IV-A and B, where we investigated samples with the same HfO_2 dielectric but with different gate electrode materials: polysilicon or metal. Comparing Figs. 3 and 6, it is clear that n-MOSFETs with polysilicon gate exhibit 1 decade larger drain noise with respect to the n-MOSFETs with metal gate. Moreover, also the GNP value in the case of polysilicon gate (Fig. 5) is 1 decade larger with respect to the one of metal gate (Fig. 8). This result further confirms the presence of a large defect density at the interface between the hafnium dioxide dielectrics and the polysilicon gates. Pantisano *et al.* [37] showed that this large amount of defects locally changes the electrostatic potential at the dielectric/gate electrode interface, causing unwanted effects such as a shift of the flatband voltage. Therefore, in the case of hafnium-based dielectrics, the interface with polysilicon strongly degrades the overall quality of the gate stack.

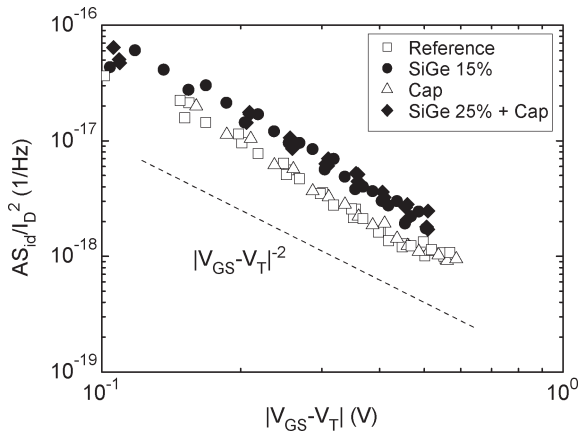


Fig. 12. Normalized drain-current spectral density at $f = 25$ Hz as a function of the gate voltage overdrive for p-MOSFETs with different strain engineering: (□) Unstressed reference, (●) 15% SiGe S/D, (△) Si_3N_4 cap layer, and (◆) 25% SiGe S/D + Si_3N_4 cap layer. In all the cases, the investigated devices were $10\ \mu\text{m}$ wide and $1\ \mu\text{m}$ long.

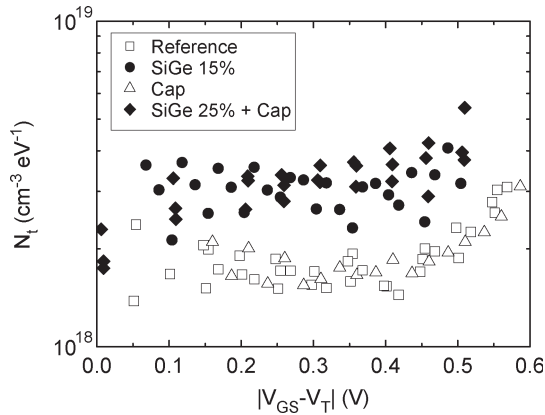


Fig. 13. Trap density for p-MOSFETs with different strain engineering. The devices were $10\ \mu\text{m}$ wide and $1\ \mu\text{m}$ long. No increase of defectivity in the gate stack is observed in the case of nitride cap layer.

D. Impact of Strain Engineering

The effect of the strain on the quality of the high- k gate dielectric was analyzed by means of drain-current noise measurements in p-MOSFET devices with different strain techniques. The gate stack of the p-MOSFETs consists of 1.8–2 nm of HfO_2 layer deposited by ALD on a 1.2–1.4-nm chemical oxide IL, resulting in an EOT of around 2.1 nm. A 4-nm-thick TiN gate electrode was fabricated by MOCVD, followed by the deposition of 100-nm polysilicon. Aside from unstressed reference devices, three different kinds of strain engineering were implemented: 15% SiGe recessed S/D regions, 100-nm nitride cap layer with 1.5-GPa compressive intrinsic stress, and a combination of recessed S/D (25% SiGe) and cap layer [38]–[41].

Comparing the normalized drain-current spectral density, some interesting trends can be found in Fig. 12. First, from the quadratic dependence of the normalized noise on the gate voltage overdrive, one can conclude that the $1/f$ noise is dictated by number fluctuations. A second clear trend is that for SiGe S/D devices, the noise is significantly higher with respect to the reference devices. Moreover, this increase is not depending on the % Ge. Third, no degradation of the noise was

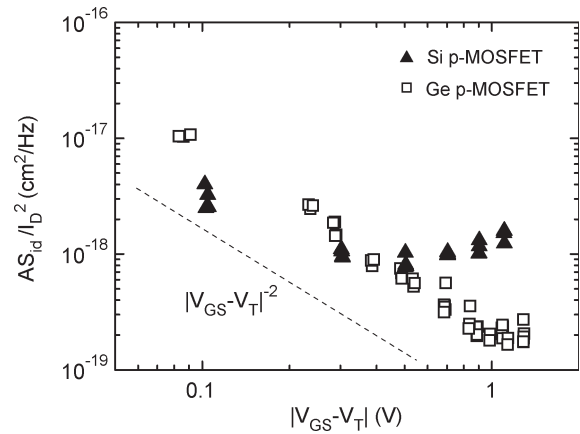


Fig. 14. Normalized drain-current spectral density at $f = 25$ Hz as a function of gate voltage overdrive for p-MOSFETs with different substrates: Silicon or germanium. For both devices, we investigated channel widths of $10\ \mu\text{m}$ and channel lengths of $1\ \mu\text{m}$. The noise seems to be slightly higher for Ge p-MOSFETs at low gate voltage overdrive.

found for the cap-only devices. The extracted trap densities are reported in Fig. 13. Here, it is possible to observe how the defect content increases when SiGe S/D strain is implemented.

From this experiment, we can conclude that it is possible to implement strain in p-MOSFETs without degradation in the high- k gate stack, by using a nitride cap layer. On the other hand, the additional selective epitaxial deposition step for fabricating the recessed SiGe S/D can induce a worsening of the quality of the high- k gate stack.

E. Impact of Substrate Material

In the last years, MOSFETs on germanium, owing to their high charge carrier mobility, are gaining interest as a replacement of the MOSFET with a silicon substrate. In order to evaluate the impact of such a new channel material on the high- k gate stack, noise properties of p-MOSFETs with Si and Ge substrates are compared in this paper when similar gate stacks are implemented. Ge p-MOSFETs were fabricated by using a standard Si-compatible process flow, and the gate stacks comprised as follows: $1.6\ \mu\text{m}$ of Ge grown by chemical vapor deposition; 0.8 nm of Si as passivation layer, partially oxidized to form a thin SiO_2 IL; HfO_2 deposited by ALD; and 10 nm of TaN capped with 100 nm of TiN for the metal gate. The Si p-MOSFET gate stack consisted of the following: SiO_2 as IL, HfO_2 as high- k gate dielectric, and TiN as metal gate. The EOT values were 1.3 and 1.2 nm for Ge MOSFETs and Si MOSFETs, respectively [42].

The drain-current noise measurements are reported in Fig. 14 where one can observe that different mechanisms generate the drain-current noise. In the case of a Si substrate, mobility fluctuation dominates, even if at high gate voltage overdrive, the normalized noise increases, probably because of the parasitic series resistance [28]. On the other hand, Ge p-MOSFETs are clearly dominated by carrier number fluctuation.

Although, in Fig. 14, only a slight increase in drain-current noise is observed in the case of Ge p-MOSFETs, in Fig. 15, the GNP for Ge p-MOSFETs is found to be more than two orders of magnitude higher with respect to the Si p-MOSFETs. Ge

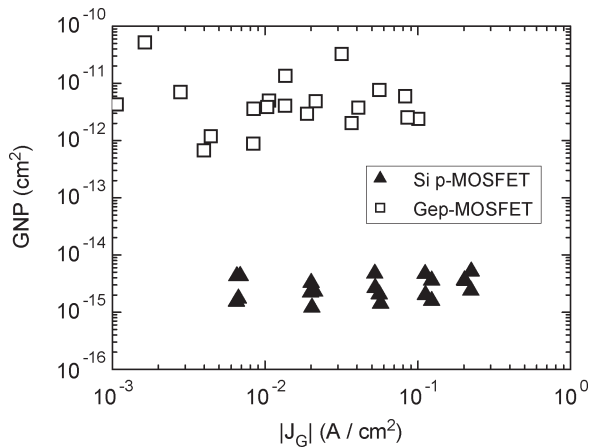


Fig. 15. GNP as a function of the gate-current density for p-MOSFETs with different substrates: Silicon and germanium. The channel widths were $10\ \mu\text{m}$, and channel lengths were $1\ \mu\text{m}$. A strong degradation of the figure of merit is observed in the case of Ge p-MOSFETs.

outdiffusion can be considered as one of the causes for the lower quality of the gate dielectric when deposited on Ge. In fact, the outdiffused Ge acts as a trap center inside the gate oxide. Hence, a higher gate-current noise is observed in Ge p-MOSFETs.

V. CONCLUSION

In this paper, we have studied the drain- and gate-current noises of MOSFET devices with high- k gate stacks. We have observed that the use of high- k dielectric such as hafnium dioxide degrades the quality of the gate stack. The trap density in the gate stack can be reduced when using other high- k dielectrics with less hafnium content, like HfSiON. In addition, we have proved that the degradation of the noise performance is not only ascribed to the kind of dielectric implemented. The IL thickness plays a significant role since the closer the high- k layer to the channel interface, the higher the noise in both drain and gate currents. Moreover, we have shown that the interface between the high- k dielectric and gate electrode is a key element in the overall quality of the gate stack. Even a submonolayer of HfO₂ sandwiched between the SiON dielectric and polysilicon gate is able to increase significantly both drain- and gate-current noises. However, much better quality of gate stack can be achieved by using a metal gate as a replacement of conventional polysilicon. We have shown that strain engineering in p-MOSFETs can be implemented by means of nitride cap layer without changing the overall quality of the high- k gate stack. The experimental results (in particular, the gate-current noise measurements) have also highlighted that in the case of a germanium channel, the quality of the high- k gate stack is degraded with respect to the silicon counterpart.

In addition to conventional noise figure of merits extracted from the drain $1/f$ noise measurements, the GNP has been used in order to characterize the quality of the gate stack from gate-current $1/f$ noise measurements. The main advantage of using the gate-current $1/f$ noise as diagnostic in MOS structures is its intrinsic immunity to the large gate leakage, which can corrupt the accuracy of all the other conventional methods. Moreover, we have seen in different experiments that the GNP value is

more sensitive to the traps far from the channel interface with respect to drain-current $1/f$ noise measurements.

REFERENCES

- [1] *International Technology Roadmap for Semiconductors*, Semicond. Ind. Assoc., San Jose, CA, 2007.
- [2] M. Houssa, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, and M. M. Heyns, "Electrical properties of high- κ gate dielectrics: Challenges, current issues, and possible solutions," *Mater. Sci. Eng.*, vol. 51, no. 4–6, pp. 37–85, 2006.
- [3] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High- κ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001.
- [4] M. Baklanov, K. Maex, and M. Green, *Dielectric Films for Advanced Microelectronics*. New York: Wiley, 2007.
- [5] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994.
- [6] R. Jayaraman and C. G. Sodini, "A $1/f$ noise technique to extract the oxide trap density near the conduction band edge of silicon," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1773–1782, Sep. 1989.
- [7] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990.
- [8] E. P. Vandamme and L. K. J. Vandamme, "Critical discussion on unified $1/f$ noise models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2146–2152, Nov. 2000.
- [9] E. Simoen, A. Mercha, L. Pantisano, C. Claeys, and E. Young, "Low-frequency noise behavior of SiO₂–HfO₂ dual-layer gate dielectric nMOSFETs with different interfacial thickness," *IEEE Trans. Electron Devices*, vol. 51, no. 5, pp. 780–784, May 2004.
- [10] J. Lee and G. Bosman, "Comprehensive noise performance of ultrathin oxide MOSFETs at low frequencies," *Solid State Electron.*, vol. 48, no. 1, pp. 61–71, Jan. 2004.
- [11] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Phys. Stat. Sol. A*, vol. 124, no. 2, pp. 571–581, 1991.
- [12] F. Martinez, C. Leyris, G. Neau, M. Valenza, A. Hoffmann, J. C. Vildeuil, E. Vincent, F. Boeuf, T. Skotnicki, M. Bidaud, D. Barge, and B. Tavel, "Oxide traps characterization of 45 nm MOS transistors by gate current R.T.S. noise measurements," *Microelectron. Eng.*, vol. 80, pp. 54–57, Jun. 2005.
- [13] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states, and low-frequency noise," *Adv. Phys.*, vol. 38, no. 4, pp. 367–468, Nov. 1989.
- [14] G. Giusi, F. Crupi, C. Pace, C. Ciofi, and G. Groeseneken, "A comparative study of drain and gate low frequency noise in nMOSFETs with hafnium based gate dielectrics," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 823–828, Apr. 2006.
- [15] P. Magnone, C. Crupi, G. Iannaccone, G. Giusi, C. Pace, E. Simoen, and C. Claeys, "A model for MOS gate stack quality evaluation based on the gate current $1/f$ noise," in *9th Int. Conf. Ultimate Integr. Silicon*, Udine, Italy, 2008, pp. 141–144.
- [16] D. K. Schroder, *Semiconductor Material and Device Characterization*. New York: Wiley, 2006.
- [17] G. Groeseneken, H. E. Maes, N. Beltràn, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, pp. 42–53, Jan. 1984.
- [18] M. B. Zahid, R. Degraeve, L. Pantisano, J. F. Zhang, and G. Groeseneken, "Defects generation in SiO₂/HfO₂ studied with variable T_{CHARGE} – T_{DISCHARGE} charge pumping (VT²CP)," in *IRPS*, 2007, pp. 55–60.
- [19] G. Giusi, F. Crupi, C. Ciofi, and C. Pace, "Instrumentation design for gate and drain low frequency noise measurements," in *Proc. IMTC Conf.*, 2006, pp. 1747–1750.
- [20] B. Min, P. Devireddy, Z. Celik-Butler, F. Wang, A. Zlotnicka, H. H. Tseng, and P. J. Tobin, "Low-frequency noise in submicrometer MOSFETs with HfO₂, HfO₂/Al₂O₃ and HfAlO_x gate stacks," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1315–1322, Aug. 2004.
- [21] G. Ghibaudo, "Low-frequency noise and fluctuations in advanced CMOS devices," in *Noise in Devices and Circuits*, vol. 5113, M. J. Deen, Z. Celik-Butler, and M. E. Levinshstein, Eds. Bellingham, WA: SPIE, 2003, pp. 16–28.
- [22] P. Morfouli, G. Ghibaudo, T. Ouisse, E. Vogel, W. Hill, V. Misra, P. McLarty, and J. J. Wortman, "Low-frequency noise characterization of n- and p-MOSFETs with ultrathin oxynitride gate films," *IEEE Electron Device Lett.*, vol. 17, no. 8, pp. 395–397, Aug. 1996.

- [23] M. Valenza, A. Hoffmann, D. Sodini, A. Laigle, F. Martinez, and D. Rigaud, "Overview of the impact of downscaling technology on 1/f noise in p-MOSFETs to 90 nm," in *Proc. Inst. Elect. Eng.—Circuits, Devices Syst.*, Apr. 2004, vol. 151, pp. 102–110.
- [24] P. Magnone, L. Pantisano, F. Crupi, L. Trojman, C. Pace, and G. Giusi, "On the impact of defects close to the gate electrode on the low-frequency 1/f noise," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1056–1058, Sep. 2008.
- [25] F. Crupi, P. Srinivasan, P. Magnone, E. Simoen, C. Pace, D. Misra, and C. Claeys, "Impact of the interfacial layer on the low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 688–691, Aug. 2006.
- [26] L.-Å. Ragnarsson, W. Tsai, A. Kerber, P. J. Chen, E. Cartier, L. Pantisano, S. De Gendt, and M. Heyns, "Mobility in high- κ dielectric based field effect transistors," in *SSDM*, 2003, pp. 46–47.
- [27] L.-Å. Ragnarsson, L. Pantisano, V. Kaushik, S.-I. Saito, Y. Shimamoto, S. De Gendt, and M. Heyns, "The impact of sub monolayers of HfO₂ on the device performance of high- k based transistors," in *IEDM Tech. Dig.*, 2003, pp. 87–90.
- [28] E. Vandamme, L. K. J. Vandamme, E. Simoen, R. Schreutelkamp, and C. Claeys, "The noise behaviour of silicided and non-silicided MOSFETs," *Solid State Electron.*, vol. 38, no. 11, pp. 1893–1897, 1995.
- [29] P. Magnone, F. Crupi, L. Pantisano, and C. Pace, "Fermi-level pinning at polycrystalline silicon-HfO₂ interface as a source of drain and gate current 1/f noise," *Appl. Phys. Lett.*, vol. 90, no. 7, pp. 073 507.1–073 507.3, Feb. 2007.
- [30] L. K. J. Vandamme, X. Li, and D. Rigaud, "1/f noise in MOS devices, mobility or number fluctuations?" *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1936–1945, Nov. 1994.
- [31] J. Chang, A. A. Abidi, and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1965–1971, Nov. 1994.
- [32] P. Magnone, C. Pace, F. Crupi, and G. Giusi, "Low frequency noise in nMOSFETs with subnanometer EOT hafnium-based gate dielectrics," *Microelectron. Reliab.*, vol. 47, no. 12, pp. 2109–2113, Dec. 2007.
- [33] M. von Haartman, G. Malm, and M. Ostling, "Comprehensive study on low-frequency noise and mobility in Si and SiGe pMOSFETs with high- κ gate dielectrics and TiN gate," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 836–843, Apr. 2006.
- [34] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani, "Unified mobility model for high- κ gate stacks," in *IEDM Tech. Dig.*, 2003, pp. 797–800.
- [35] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high- κ insulator: The role of remote phonon scattering," *J. Appl. Phys.*, vol. 90, no. 9, pp. 4587–4608, Nov. 2001.
- [36] Z. Ren, M. V. Fischetti, E. P. Gusev, E. A. Cartier, and M. Chudzik, "Inversion channel mobility in high- κ high performance MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 793–796.
- [37] L. Pantisano, V. Afanas'ev, G. Pourtois, and P. J. Chen, "Valence-band electron-tunneling measurement of the gate work function: Application to the high- k /polycrystalline-silicon interface," *J. Appl. Phys.*, vol. 98, no. 5, pp. 053 712-1–053 712-8, Sep. 2005.
- [38] G. Eneman, M. Jurczak, P. Verheyen, T. Hoffmann, A. De Keersgieter, and K. De Meyer, "Scalability of strained nitride capping layers for future CMOS generation," in *Proc. ESSDERC*, Grenoble, France, 2005, pp. 449–453.
- [39] P. Verheyen, G. Eneman, R. Rooyackers, R. Loo, L. Eeckhout, D. Rondas, F. Leys, J. Snow, D. Shamiryman, M. Demand, T. Y. Hoffmann, M. Goodwin, H. Fujimoto, C. Ravit, B.-C. Lee, M. Caymax, K. De Meyer, P. Absil, M. Jurczak, and S. Biesemans, "Demonstration of recessed SiGe S/D and inserted metal gate on HfO₂ for high performance pMOSFETs," in *IEDM Tech. Dig.*, 2005, pp. 907–910.
- [40] C. Claeys, E. Simoen, S. Put, G. Giusi, and F. Crupi, "Impact strain engineering on gate stack quality and reliability," *Solid State Electron.*, vol. 52, no. 8, pp. 1115–1126, Aug. 2008.
- [41] G. Giusi, E. Simoen, G. Eneman, P. Verheyen, F. Crupi, K. De Meyer, C. Claeys, and C. Ciofi, "Low-frequency (1/f) noise behavior of locally stressed HfO₂/TiN gate-stack pMOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 6, pp. 508–510, Jun. 2006.
- [42] D. Maji, F. Crupi, G. Giusi, C. Pace, E. Simoen, C. Claeys, and V. R. Rao, "On the DC and noise properties of the gate current in epitaxial Ge p-channel metal oxide semiconductor field effect transistors with TiN/TaN/HfO₂/SiO₂ gate stack," *Appl. Phys. Lett.*, vol. 92, no. 16, p. 163 508.1, 2008.



P. Magnone received the B.S. and M.S. degrees in electronic engineering from the University of Calabria, Cosenza, Italy, in 2003 and 2005, respectively, and the Ph.D. degree in electronic engineering from the University of Reggio Calabria, Reggio Calabria, Italy, in 2009.

From 2006 to 2008, he was with the Interuniversity Micro-Electronics Center, Leuven, Belgium, within the APROTHIN project (Marie Curie Actions), where he worked on parameters extraction and matching analysis of FinFET devices. He is currently a Postdoctoral Researcher with the Dipartimento di Elettronica, Informatica e Sistemistica, University of Calabria. His research interests include the electrical characterization of semiconductor devices with particular emphasis on the study of low-frequency noise.



F. Crupi received the M.Sc. degree in electronic engineering from the University of Messina, Messina, Italy, in 1997 and the Ph.D. degree from the University of Firenze, Firenze, Italy, in 2001.

Since 2002, he has been with the Dipartimento di Elettronica, Informatica e Sistemistica, University of Calabria, Cosenza, Italy, where he is currently an Associate Professor of electronics. Since 1998, he has been a repeat Visiting Scientist with the Interuniversity Micro-Electronics Center, Leuven, Belgium. In 2000, he was a Visiting Scientist with the IBM

Thomas J. Watson Research Center, Yorktown Heights, NY. In 2006, he was a Visiting Scientist with the Universitat Autònoma de Barcelona, Barcelona, Spain. He is the author or a coauthor of more than 100 publications in international scientific journals and international conference proceedings. His main research interests include reliability of very large scale integration CMOS devices, electrical characterization techniques for solid-state electronic devices, and the design of ultralow-noise electronic instrumentation.



G. Giusi received the M.Sc. and Ph.D. degrees in electronic engineering from the University of Messina, Messina, Italy, in 2002 and 2005, respectively.

In 2005, he was a Visitor with the Interuniversity Micro-Electronics Center, Leuven, Belgium. In 2006, he was with the National Research Center, Catania, Italy. He is currently a Contract Researcher and a Contract Professor with the Dipartimento di Elettronica, Informatica e Sistemistica, University of Calabria, Cosenza, Italy. He is the author of more

than 20 papers in international journals. His main research interests include the study of electrical characterization techniques and reliability for solid-state electronic devices, the modeling and simulation of nanoscale CMOS transistors and memories, and the design of ultralow-noise electronic instrumentation and techniques for low-frequency noise measurements.

Dr. Giusi serves as a Reviewer for the IEEE TRANSACTIONS ON ELECTRON DEVICES and IEEE ELECTRON DEVICE LETTERS.



C. Pace received the M.Sc. and Ph.D. degrees in electronic engineering from the University of Palermo, Palermo, Italy, in 1990 and 1994, respectively.

In 1996, he was with the University of Messina, Messina, Italy, as an Assistant Professor. In 2002, he joined the Dipartimento di Elettronica, Informatica e Sistemistica, University of Calabria, Cosenza, Italy, where he is currently an Associate Professor of electronics. He coordinated the Italian Ministry of Foreign Affairs international project "RHESSA" on the radiation hardness of electronic devices and

systems for space applications. He is a coauthor of about 40 scientific and technical papers published in international refereed journals. He is currently involved in research projects on the design of low-noise electronic instrumentation, the design and characterization of electronic gas sensors, and the study of nanocrystal and SONOS memory devices.



E. Simoen received the Master's degree in physics engineering and the D.Eng. degree from the University of Gent, Gent, Belgium, in 1980 and 1985, respectively. His doctoral thesis was devoted to the study of trap levels in high-purity germanium by deep-level transient spectroscopy.

In 1986, he joined the Interuniversity Micro-Electronics Center (IMEC), Leuven, Belgium, working in the field of low-temperature electronics. He is an IMEC Scientist, currently involved in the study of defect and strain engineering in high-mobility and epitaxial substrates and defect studies in germanium. He is the author or a coauthor of more than 1000 journal and conference papers, 11 book chapters, and a monograph entitled *Radiation Effects in Advanced Semiconductor Devices and Materials* (Springer, 2002), whose Chinese translation has been published in March 2008. He was also a Coeditor of the book *Germanium-Based Technologies: From Materials to Devices* (Elsevier, March 2007) and a new book *Fundamental and Technological Aspects of Extended Defects in Germanium* (Springer, January 2009). He acted as a Coeditor of four international conference proceedings. His current interests cover the field of device physics and defect engineering in general, with particular emphasis on the study of low-frequency noise, low-temperature behavior, and radiation defects in semiconductor components and materials.

Dr. Simoen was a Lecturer at the International Noise School held at IMEC in 1993, at the European Network on Defect Engineering of Advance Semiconductor Devices Workshop in Santorini, Greece, in April 1999 and in Stockholm, Sweden, in June 2000, and at the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EUROSOI) Workshop in Leuven in January 2007.



C. Claeys (M'94-SM'95-F'09) received the Master degree in electrical-mechanical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven (KU Leuven), Leuven, Belgium, in 1974 and 1979, respectively.

From 1974 to 1984, he was a Research Assistant and then a Staff Member with the Department of Electrical Engineering, KU Leuven, where he has been a Professor since 1990. In 1984, he joined the Interuniversity Micro-Electronics Center, Leuven, as the Head of the Silicon Processing Group. Since 1990, he has been the Head of the Research Group on Radiation Effects, Cryogenic Electronics, and Noise Studies. Recently, he became as the Director Advanced Semiconductor Technologies, being responsible for strategic relations. He is also a member of the European Expert Group on Nanosciences. He had short stays as a Visiting Professor with Queens University, Belfast, Ireland, and the University of Calabria, Cosenza, Italy. He is a Coeditor of a book on low-temperature electronics and the book *Germanium-Based Technologies: From Materials to Devices* (Elsevier, March 2007). He is the author of the monographs *Radiation Effects in Advanced Semiconductor Materials and Devices* (Springer, 2002) and *Fundamental and Technological Aspects of Extended Defects in Germanium* (Springer, January 2009). He is also the author or a coauthor of eight book chapters and more than 800 technical papers and conference contributions. He has been involved in the organization of a large number of international conferences and edited more than 40 proceedings volumes. He is an Associated Editor for the *Journal of the Electrochemical Society*. His main interests are, in general, silicon technology for ULSI, device physics, including low-temperature operation, low-frequency noise phenomena and radiation effects, and defect engineering and material characterization.

Dr. Claeys is a Fellow the Electrochemical Society. He was the Founder of the IEEE Electron Devices Benelux Chapter, the Chair of the IEEE Benelux Section, an Elected Administrative Committee Member of the Electron Devices Society (EDS) from 1999 to 2005, and the EDS Vice President for Chapters and Regions from 2000 to 2006. Since 2000, he has been an EDS Distinguished Lecturer. He was elected as the EDS President-Elect in 2006 and became the EDS President in 2008. Within the Electrochemical Society, he has been serving in different committees and was the Chair of the Electronics Division from 2001 to 2003. In 1999, he was elected as an Academician and Professor of the International Information Academy. He is the recipient of the IEEE Third Millennium Medal. In 2004, he received the Electronics Division Award of the Electrochemical Society.



L. Pantisano received the M.S. and Ph.D. degrees in electrical engineering from the University of Padova, Padova, Italy, in 1996 and 2000, respectively.

In 2000, he was with Bell Laboratories, Lucent Technologies, Murray Hill, NJ, pursuing the impact of plasma-charging damage on RF CMOS devices. Since 2001, he has been with the Interuniversity Micro-Electronics Center, Leuven, Belgium, working on high- k gate dielectrics for CMOS and memory technologies. He is the author of more than 150 papers in the field of plasma damage, RF measurements, reliability, and electrical characterization of novel high- k devices.

Dr. Pantisano is a committee member of several conferences, namely, IEEE Semiconductor Interface Specialists Conference (SISC), IEEE International Reliability Physics Symposium (IRPS), IGSAT, and International Conference on Microelectronic Test Structures (ICMTS).



D. Maji received the B.Tech and M.Tech degrees in radiophysics and electronics from the University of Calcutta, Kolkata, India in 2001 and 2003, respectively. He is currently working toward the Ph.D. degree with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India.

In 2006, he was a Summer Intern Researcher with the Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan. In 2008, he was a Visiting Indian Researcher with the University of Calabria, Cosenza, Italy. His research interests include device characterization, reliability, and noise measurement in advance MOS devices.



V. Ramgopal Rao (M'98-SM'02) received the M.Tech. degree from the Indian Institute of Technology (IIT), Bombay, Mumbai, India, in 1991 and the Dr.Ing. degree from the Universitaet der Bundeswehr Munich, Germany, in 1997.

From 1997 to 1998 and again in 2001, he was a Visiting Scholar with the Electrical Engineering Department, University of California, Los Angeles. He is currently a Professor with the Department of Electrical Engineering, IIT Bombay. He is the Chief Investigator for the Centre for Excellence in Nanoelectronics project at IIT Bombay in addition to being the Principal Investigator for many ongoing sponsored projects funded by various multinational industries and government agencies. He also serves on various Government of India committees on nanotechnology. He is the author of more than 200 publications in refereed international journals and conference proceedings. He is the holder of three patents, with seven currently pending. His research interests include physics, technology, and characterization of silicon CMOS devices for logic and mixed-signal application and nanoelectronics.

Prof. Rao is a Fellow of the Indian National Academy of Engineering, the Indian Academy of Sciences, and the Institution of Electronics and Telecommunication Engineers. He is an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES in the CMOS devices and technology area and is a Distinguished Lecturer of the IEEE Electron Devices Society. He was the Organizing Committee Chair for the Seventeenth International Conference on VLSI Design and the Fourteenth International Workshop on the Physics of Semiconductor Devices and serves on the program/organizing committees of various international conferences, including the International Electron Devices Meeting, IEEE Asian Solid-State Circuits Conference, 2006 IEEE Conference on NanoNetworks, ACM/IEEE International Symposium on Low Power Electronics and Design, Eleventh IEEE VLSI Design and Test Symposium. He was the Chairman of the IEEE AP/ED Bombay Chapter during 2002–2003 and currently serves on the executive committee of the IEEE Bombay Section in addition to being the Vice Chair of the IEEE Asia-Pacific Regions/Chapters Subcommittee. He received the Shanti Swarup Bhatnagar Prize in Engineering Sciences in 2005 for his work on electron devices. He also received the Swarnajayanti Fellowship Award for 2003–2004, instituted by the Department of Science and Technology, Government of India, the 2007 IBM Faculty Award, and the 2008 "The Materials Research Society of India (MRSI) Superconductivity & Materials Science Prize."



P. Srinivasan received the Ph.D. degree from the Interuniversity Micro-Electronics Center (IMEC), Leuven, Belgium, and the New Jersey Institute of Technology, Newark, in 2007. His doctoral dissertation was focused on $1/f$ low-frequency noise in high- k dielectrics for 45-nm nodes and below.

He was a Researcher with the IBM T. J. Watson Research Center, Yorktown Heights, NY, in the summer of 2006. Since 2007, he has been a Low-Frequency Noise Test and Characterization Engineer with the Spice Modeling Group of Technology Design Integration Team, External Development and Manufacturing Group, Texas Instruments Incorporated, Dallas, TX. He is the author or a coauthor of more than 15 papers in journal publications and 25 papers in international conference proceedings.

Dr. Srinivasan received the Hashimoto Prize for best doctoral dissertation in 2007.