NBTI Degradation and Its Impact for Analog Circuit Reliability

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***Abstract*—A methodology to quantify the degradation at circuit level due to negative bias temperature instability (NBTI) has been proposed in this work. Using this approach, a variety of analog/mixed-signal circuits are simulated, and their degradation is analyzed. It has been shown that the degradation in circuit performance is mainly dependent on the circuit configuration and its application rather than the absolute value of degradation at the device level. In circuits such as digital-to-analog converters, NBTI can pose a serious reliability concern, as even a small variation in bias currents can cause significant gain errors.**

***Index Terms*—Analog/mixed-signal circuits, circuit lifetime, negative bias temperature instability (NBTI), pMOSFET degradation, threshold-voltage shift.**

I. Introduction

NEGATIVE bias temperature instability (NBTI) occurs in p-channel MOS devices stressed with negative gate bias at elevated temperatures. The impact of NBTI degradation on MOS circuit behavior is generally studied for digital circuit performance degradation [1]–[8], as digital circuits are usually subjected to enhanced gate and drain voltages which are comparable to the supply voltage. In addition to digital circuits, NBTI is reported to be a major reliability concern for analog circuits as has been shown by device-level characterizations for various analog performance parameters [9]–[12]. This is primarily due to the recent introduction of surface-channel pMOSFETs for analog circuits [6], [13], as most of the circuit blocks (digital and analog) are fabricated on the same chip for system-on-chip (SOC) applications.

NBTI degradation in MOSFETs is explained by the reaction-diffusion model mentioned in [14]–[19]. According to the standard reaction–diffusion (RD) model for NBTI, for a negatively biased pMOS transistor, the holes in the inversion layer react with the Si-H bonds at the Si/SiO_2 interface. This leads to the dissociation of the Si-H bonds and results in Si- dangling bonds at the interface. The generated hydrogen species diffuse away from the interface toward the polysilicon gate. In the absence of holes near the interface, a reverse reaction takes place in which hydrogen species diffuse back to the Si/SiO_2 interface and react with Si- bonds to anneal the generated interface states [20]–[24]. For this reason, it is important to take into account the effect of annealing in the circuit-level degradation studies. It has also been shown recently that the digital circuit lifetime, determined by static NBTI degradation, greatly underestimates the actual circuit lifetime by overlooking the electrical passivation during normal operation of digital circuits [21]. The NBTI reverse reaction, during low output phase of an inverter, has been postulated as a reason for electrical passivation and subsequent recovery of NBTI degradation in pMOSFETs [22]–[24]. The NBTI degradation study at dynamic stress conditions and subsequent frequency dependence suggests almost a complete anneal of NBTI degradation and an overly enhanced lifetime for digital circuits [20], [21], [23]. A postrecovery response of stress is critical in digital circuits, as a continuous dc stress is seldom seen. In the case of analog circuits, dc biasing voltages always exist irrespective of the input signal. In addition to the applied dc gate and drain voltages, a high temperature may also exist on the chip because of the high-density digital circuitry on the same chip. This would result in a continuous NBTI stress in analog circuits but with minor electrical passivation and subsequent anneal.

NBTI is a significant concern for analog circuits since many analog operations require matched device pairs and mismatches induced by NBTI could cause circuit failure. Typically, time-zero mismatch in paired devices is minimized by techniques like common-centroid layout. It has been observed that the parametric shift in pMOS devices due to NBTI can be significantly higher than the desired zero-time matching. Usually, a percentage change in I_{Dsat} is defined as a parametric failure for analog circuit operations [9]. Although analog circuits are not subjected to high gate and drain bias voltages during circuit operation, less tolerance (in some circuits) and continuous dc stress can impose a fundamental limit to the analog circuit reliability due to NBTI.

In this paper, a detailed investigation of the threshold voltage degradation and the consequent BSIM parameter variation is used to study the effect of NBTI on analog circuit reliability. The implication of NBTI stress on different analog circuit topologies is systematically investigated for the first time as part of this work.

II. Device Fabrication and Experiment

The devices studied in this work are p-channel conventional MOSFETs fabricated using bulk CMOS technology. Gate oxide (3.8 nm) was grown in dry O_2 followed by *in situ* N_2O anneal. Shallow SDE regions were formed using BF_2 implantation. The p-channel MOSFETs used in this study have p^+ poly Si gate; a PMA in forming gas was performed on all devices. The stress measurements are performed on pMOS devices. Stressing was done at logarithmic time intervals, which were interrupted periodically to measure $I_{\mathrm{d}} - V_{\mathrm{gs}}$ and charge-pumping current.

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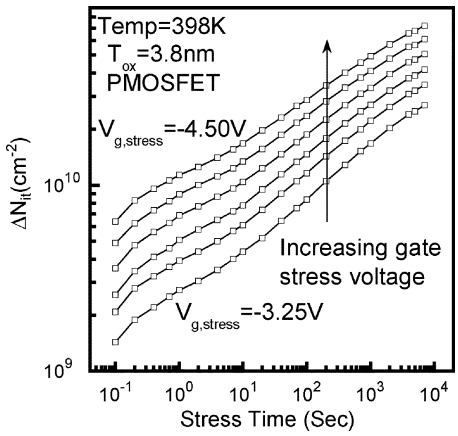

Fig. 1. Time evolution of interface state generation for the pMOS devices stressed at various gate voltages.

The measurements were used to monitor the changes in the gate threshold voltage $V_{\rm th}$) and interface-state density $(N_{\rm it})$. The applied gate stress $(V_{g,\rm stress})$ ranges from -3.0 to -5.0 V. Channel lengths of the devices ranged from 0.16–2 μm. The stress and measurement temperatures were varied from 25 °C to 150 °C. The degradation of pMOSFET $(\Delta V_{\rm th})$ is observed from a shift in gate voltage which gives a drain current of 0.1 μA $*$ W/L. After each stress duration, threshold voltage shift and charge pumping $(I_{\rm CP})$ current measurements were performed to determine the generated oxide charge and interface states. To minimize the measurement delay between two successive stress points, charge pumping currents were measured at a fixed pulse height, and threshold voltages were measured by taking a few $I_{\rm d} - V_{\rm gs}$ data points at $V_{\rm d} = -0.1$ V close to the initial $V_{\rm th}$. The charge pumping $(I_{\rm CP})$ current and threshold voltage degradation measurements are performed on identically stressed different pMOSFETs.

III. Experimental Results

A. Device Degradation Due to NBTI

The negative bias temperature stressed threshold voltage degradation for pMOSFETs as a function of time is shown in Fig. 1. The threshold voltage $(V_{\rm th})$ degradation of pMOSFETs shows a time-dependent exponential in the range of 0.20–0.25. The applied stress gate voltages are scaled to result in an oxide field in the range of 5–9 MV/cm. Usually, the transistors in an analog circuit are operated with effective gate voltages $(V_{\rm eff} = V_{\rm gs} - V_{\rm th})$ of several hundred millivolts to ensure the required input signal swing and the linearity. Further, for system-on-chip (SoC) applications, high temperatures may exist on the chip due to the high package density, which aggravates the NBTI. This causes a considerable shift in threshold voltages at normal analog operating voltages. As we shall show in this work, less tolerance (in some circuits) and continuous dc stress can impose a fundamental limit to the analog circuit reliability due to NBTI. For short channel devices, the stress conditions might result in nonuniform or inhomogeneous degradation along the channel [25], but for longer channel cases this inhomogeneous degradation is negligible [26]. So, one can assume a uniform degradation along the channel length. The analog device operation could also result in channel

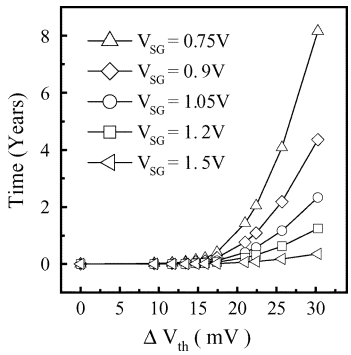

Fig. 2. Operational time as a function of threshold voltage variation $(\Delta V_{\rm th})$ for different operating voltages at $T = 125$ °C. Here $V_{\rm SG}$ represents the source-gate voltage for the pMOS device.

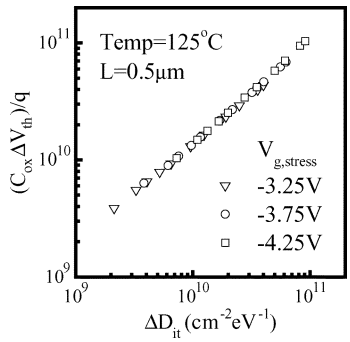

Fig. 3. Correlation of threshold voltage degradation to interface state generation for 3.8-nm oxide pMOSFETs stressed at $T = 125$ °C and various gate stress voltages.

hot carrier (CHC) stress in addition to NBTI stress, but it has been observed that degradation due to NBTI is much more compared to degradation due to CHC for the temperatures, oxide thickness, and channel lengths involved [26]. The scaled time dependencies of a pMOS transistor at different operating voltages are shown in Fig. 2. The $V_{\rm th}$ degradation in Fig. 2 is extrapolated by scaling the gate voltages to the typical analog operating voltages. The extrapolation is done by using

$$\Delta V_{\rm th} = A \exp(\beta V_G) \exp\left(\frac{-Ea}{KT}\right) t^n \qquad (1)$$

where A, E_a, and β are the experimentally determined fitting parameters. E_a is calculated to be 0.145 eV and β is 0.75 for the devices under study. It has been found that n varies between 0.19$\sim$0.26 for the devices under study. Equation (1) is formulated by considering that NBTI is dependent on hole density and the hole tunneling probability at the interface. The field-dependent tunneling probability is proportional to $\exp(E_{\rm ox})$ [15], [27]. Assuming that degradation mechanism explained by reaction-diffusion (RD) equations holds at all gate voltages, the extrapolation technique gives an estimate of the device degradation with time under analog operating conditions. Fig. 3 shows the correlation between $\Delta V_{\rm th}$ to $\Delta D_{\rm it}$, and as can be inferred from this data, the contribution of oxide traps $(\Delta N_{\rm ot})$ to the threshold voltage degradation is around 20%–25%. It has also been reported that oxide trap generation $(\Delta N_{\rm ot})$ is gate voltage dependent with higher oxide trap generation taking place at higher gate stress biases [18]. Hence, for the relatively lower gate voltages under analog conditions, one can expect to see

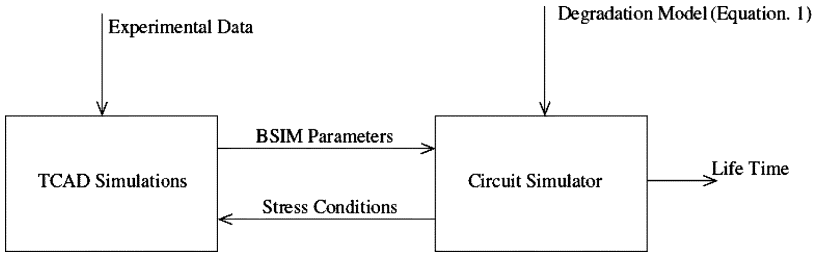

Fig. 4. Block diagram which illustrates the methodology to evaluate the impact of NBTI on analog circuits.

threshold voltage degradation mainly due to interface state generation. Consequently, the threshold voltage degradation due to interface state generation can be written by the following equation:

$$\Delta N_{\rm it} \approx \frac{\Delta V_{\rm th} C_{\rm ox}}{q}. \tag{2}$$

B. Simulation Methodology for Reliability Estimation

The effect of NBTI degradation at circuit level has been evaluated using the stressed device degradation data and the unstressed BSIM3v3.1 parameters extracted for the experimental devices under study. For a stressed MOS device, the BSIM parameter extraction involves a delay of few hundreds of seconds which would result in the annealing of generated interface traps and hence would give an incorrect set of BSIM parameters for negative bias stressed pMOSFETs. Therefore, to estimate the analog circuit degradation independent of annealing, MOSFETs having same process parameters as of the experimental devices are simulated using process simulations DIOS-ISETCAD [28] and the output characteristics of the simulated devices are matched with those of experimental devices. The motivation behind the whole exercise is to create test structures for extracting the BSIM parameters without taking into account the parameter variation due to device annealing during BSIM parameter extraction. Using this experimental data and the ISE-TCAD simulation routines for BSIM parameter extraction, the BSIM parameters were evaluated at different stress times for circuit simulations.

The circuit reliability estimation methodology followed in this work using the device stress characterization data is illustrated in the form of a block diagram in Fig. 4. Since different transistors in the circuit are biased differently, they also undergo different amounts of degradation during the circuit operation. This aspect is taken into account with the help of a generalized device degradation model [given in (1)], which is used to predict the different amounts of degradation for devices in a circuit. The circuit of interest is initially simulated with unstressed BSIM parameters and the bias voltages so generated are used to obtain the NBTI degradation (drift in $V_{\rm th}$) in the device parameters. Threshold voltage shift is correlated to interface states by (2) and the subsequent degraded device is re-simulated to extract a new set of BSIM parameters. Using this degradation data, BSIM parameters are generated using TCAD simulations and the circuit is simulated once again to observe the degradation as well as the new operating conditions. The degradation data is generated at logarithmic time intervals and the difference between two successive time steps has been kept small enough that the variation in bias conditions over the period is not significant. For each set of degradation data, a new set of BSIM parameters are extracted using TCAD simulations, which are used to study the circuit performance degradation using SPICE under the NBTI stress. The methodology explained above takes into account the degradation in both $V_{\rm th}$ and mobility (μ) because of interface state generation as pMOSFETs are simulated with appropriate mobility models. This methodology has been used to study the effect of device degradation due to NBTI on various circuits such as current mirrors, comparator, op-amp, and digital-to-analog converter (DAC).

IV. Circuit Degradation Due to NBTI

A. Current Mirrors

Analog integrated circuits often employ a constant current biasing scheme using current mirrors. As a consequence, drifts in the bias currents can cause a significant deviation in the performance of an analog circuit. So, a variety of current mirrors (shown in Fig. 5) were simulated using the above approach to see the amount of drift in bias currents as a function of NBTI-induced $V_{\rm th}$ degradation. For sake of a fair comparison, all the circuits shown in Fig. 5 were designed for a bias current $(I_{\rm bias})$ of 200 μA and the effective gate voltages $(V_{\rm geff})$ for all the devices were kept around 0.3 V. The value of V_o in each case was adjusted to keep all the transistors in saturation and to pull a current equal to $I_{\rm bias}$.

In Fig. 5, three different current mirror configurations are presented which are analyzed for their NBTI performance. Fig. 5(a) is a simple current mirror, which is used in applications where a very high-output resistance is not needed. The circuit shown in Fig. 5(b) is a cascode current mirror, which has higher output impedance compared to a simple current mirror. Finally, the circuit in Fig. 5(c) is a constant g_m biasing circuit and is used in applications where stable transconductances are required [29]. In this circuit, a positive feedback is always maintained to match all the transconductances to the conductance of a resistor (R). Because of this reason, as long as the resistance (R) is constant, the bias currents are maintained at a constant value irrespective of the variations in $V_{\rm th}$, temperature, and supply voltage. Fig. 6 shows the variation of currents in the simple current mirror [shown in Fig. 5(a)] as a function of NBTI-induced $\Delta V_{\rm th}$. As the two transistors M_1 and M_2 undergo identical gate stress voltage, $\Delta V_{\rm th}$ will vary identically for both of them. It is clear from Fig. 6 (left axis) that the output current $(I(V_{\rm o}))$ follows the bias current $(I_{\rm bias})$ for the $\Delta V_{\rm th}$ range considered. In Fig. 6 (right axis) the variation in gate-to-source voltage $(V_{\rm SG})$ for transistors M_1 and M_2 is plotted during the NBTI stress. As can be seen, the NBTI degradation causes a further increase in stress

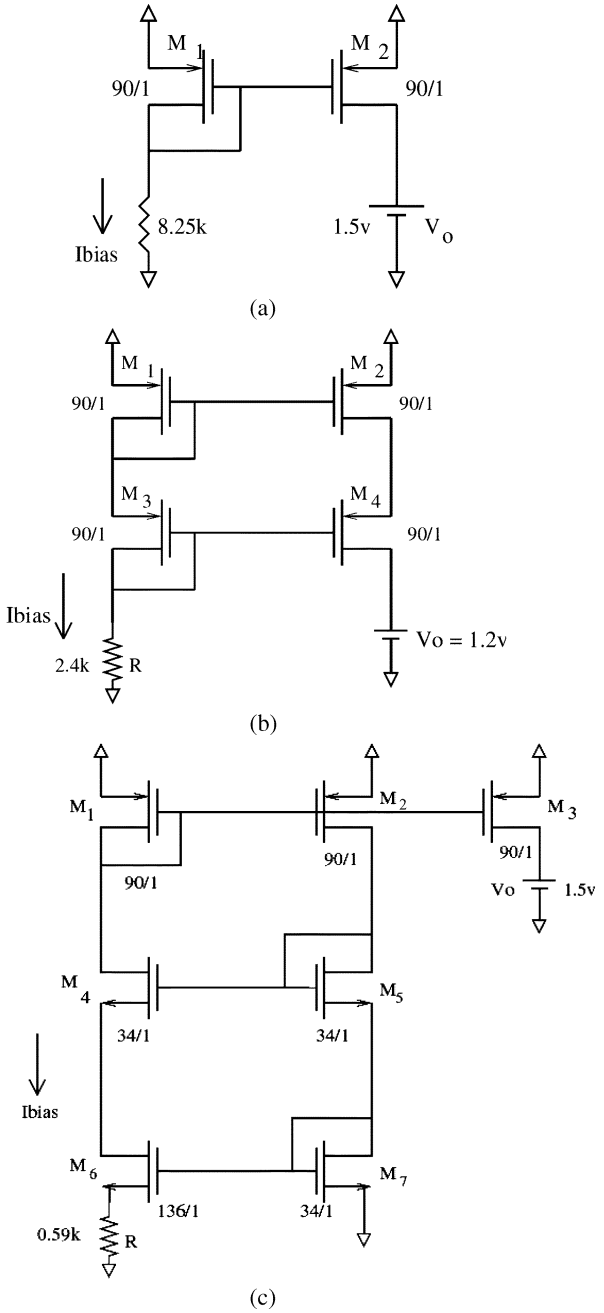

Fig. 5. SPICE simulated different current biasing circuits to study the effect of device degradation on circuit performance. All dimensions are in microns. The bias current ($I_{\rm bias}$) is 200 μA in all the circuits. The circuits are (a) simple current mirror, (b) cascode current mirror and, (c) wide-swing current mirror biasing circuit.

voltages, which therefore must be taken into account for lifetime prediction of circuits. Fig. 7 shows a comparison between SPICE and mixed-mode simulations (in ISETCAD) for the circuit in Fig. 5(a). An excellent match between the SPICE and mixed-mode simulations brings out the validity of our approach. In Fig. 8 we compare the reliability performance of the three different types of current mirror circuits shown in Fig. 5. As shown in Fig. 8, the cascode current mirror [Fig. 5(b)] shows the maximum drift ($\sim$12.5%) in the output current for the same amount of NBTI-induced $\Delta V_{\rm th}$ degradation, while the constant g_m biasing circuit [Fig. 5(c)] shows the least degradation ($<$1%). The highest degradation in the cascode current mirror can be ex-

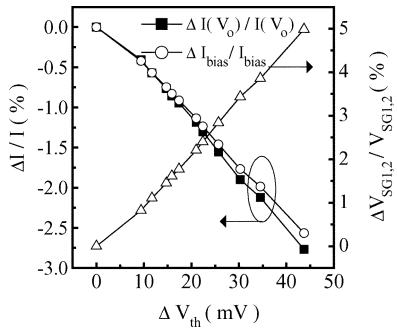

Fig. 6. Drifts in (left axis) operating currents and (right axis) voltages as a function of $\Delta V_{\rm th}$. The o/p current almost follows the bias current for the given $\Delta V_{\rm th}$ range with a 5% increase in the operating voltages.

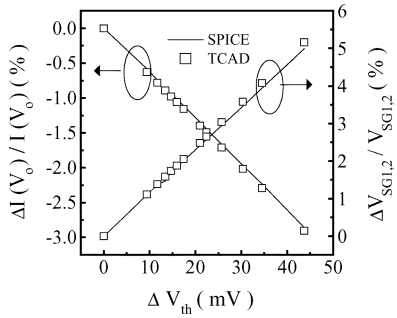

Fig. 7. Comparison of SPICE and mixed-mode simulations for the current biasing circuit shown in Fig. 4(a). Mixed-mode simulations are performed in DESSIS-ISETCAD. An excellent match between our approach for circuit reliability estimation and the mixed-mode simulations is observed.

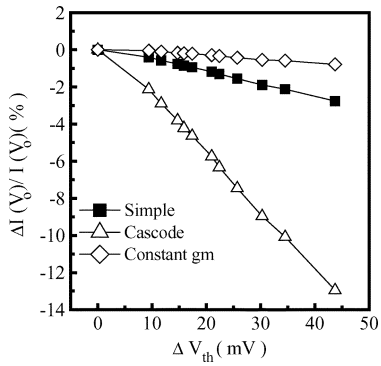

Fig. 8. Comparison showing the drifts in output currents for various biasing circuits shown in Fig. 4. The observed current variation is different for various circuits under study for the same amount of NBTI-induced $\Delta V_{\rm th}$ degradation.

plained by considering that there are two diode connected transistors in series and hence the change in voltage across the biasing resistor is a result of change in the $V_{\rm th}$'s of two transistors (M_1 andM_3). The least degradation observed in the constant g_m biasing circuit [Fig. 5(c)] is a result of the positive feedback, which takes care of the $V_{\rm th}$ variation due to NBTI. However, as we shall show in the later part of this paper, in circuits like DACs, even a 1% variation in the biasing currents can cause significant drift in the output characteristics. It is, therefore, clear from Fig. 8 that for the same amount of $V_{\rm th}$ variation due to NBTI, different current mirror configurations behave differently and hence must be chosen depending on the application.

B. Operational Amplifier

The schematic shown in Fig. 9 is a simple two-stage CMOS operational amplifier. The circuit was designed for the specifica-

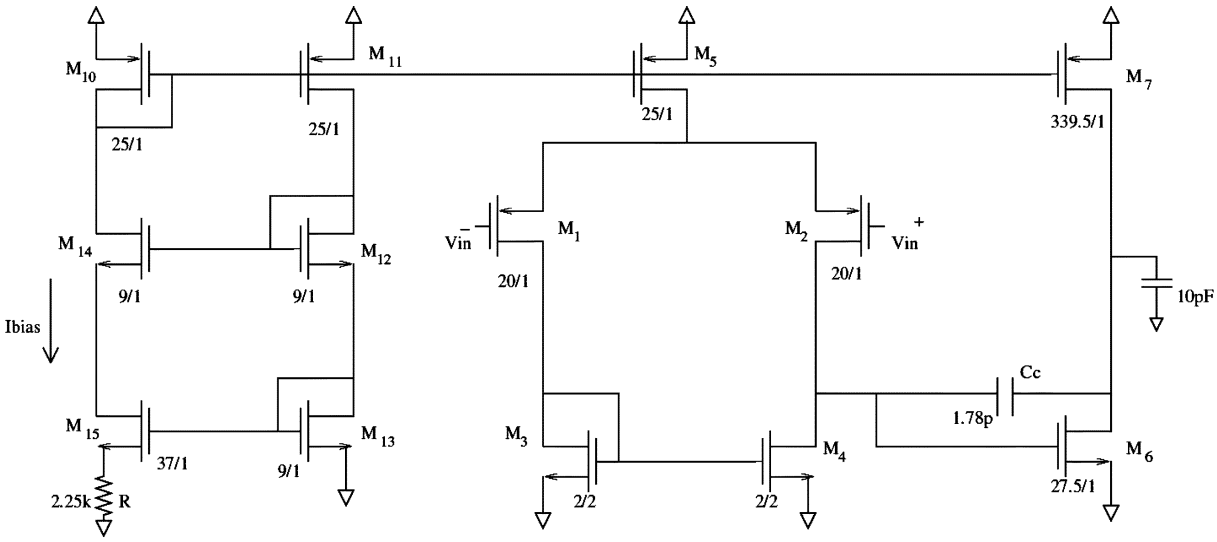

Fig. 9. Two-stage CMOS operational amplifier, simulated in SPICE. The parameter specifications are given in Table I. All dimensions are in microns.

TABLE I
TWO-STAGE CMOS OPAMP PARAMETER SPECIFICATIONS. THE CIRCUIT DIAGRAM IS SHOWN IN FIG. 8

Parameter Specifications	Value
DC Gain (A_{vo})	74dB
ICMR	0.55-1.4 V
Slew Rate	30 V/μs
Unity Gain Frequency (f_T)	16 MHz
Phase Margin	51°

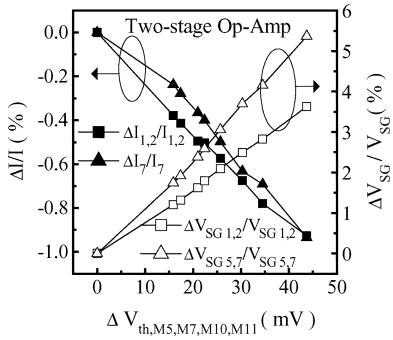

Fig. 10. Variations in dc operating conditions as a function of $\Delta V_{\rm th}$ for the two-stage op-amp shown in Fig. 8. No significant change is observed in the biasing currents.

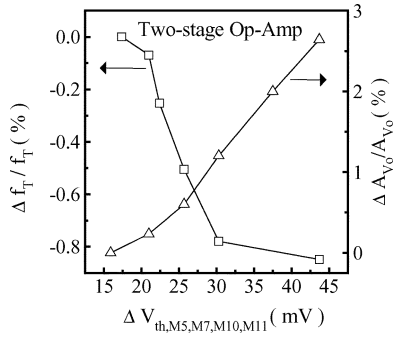

Fig. 11. Variations in (left axis) unity gain frequency and (right axis) dc gain due to $\Delta V_{\rm th}$ degradation. A 3% increase in gain is observed due to the reduction in bias currents.

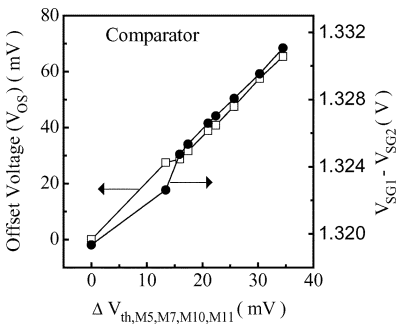

Fig. 12. Input referred offset voltage variation of circuit shown in Fig. 8 as a function of $\Delta V_{\rm th}$ (left axis). The analysis is done by biasing the gate of M_1 to $V_{\rm DD}/2$ and the gate of M_2 to ground. The difference between the stress voltages is also plotted (right axis).

tions mentioned in Table I. The circuit was simulated to see the variations in dc biasing currents because of NBTI-induced $V_{\rm th}$ degradation. As the transistors M_{10}, M_{11}, M_5, and M_7 undergo identical gate voltage stressing, $V_{\rm th}$ for them degrades identically. However, the input transistor pair M_1 and M_2 undergoes a higher amount of stress because of the body effect, since the bodies of these transistors are tied to the supply voltage. Fig. 10 shows the variations in bias currents and bias voltages because of $V_{\rm th}$ variations in M_5, M_7, M_{10} and M_{11}. Similarly variations in dc gain $(A_{\rm vo})$ and the unity gain frequency (f_T) are shown in Fig. 11. Interestingly an increase in $A_{\rm vo}$ of about 3% has been observed due to the reduction in bias currents. Thus, the two-stage op-amp did not show a significant deviation in its parameters for the $\Delta V_{\rm th}$ range considered in this work. This can be explained from the fact that the constant g_m biasing circuit employed in the op-amp keeps the biasing currents constant, by adjusting the gate voltages, when there is an NBTI-induced shift in the threshold voltage.

C. Comparator

The op-amp circuit in Fig. 9 is also simulated as a comparator with unequal stressing voltages on M_1 and M_2 to see the variations in input referred offset voltage $(V_{\rm OS})$. In this analysis the negative terminal $V_{\rm in}^-$ (gate of M_1) is kept fixed at $V_{\rm DD}/2$, and the other terminal (gate of M_2) is varied from 0 to $V_{\rm DD}$.

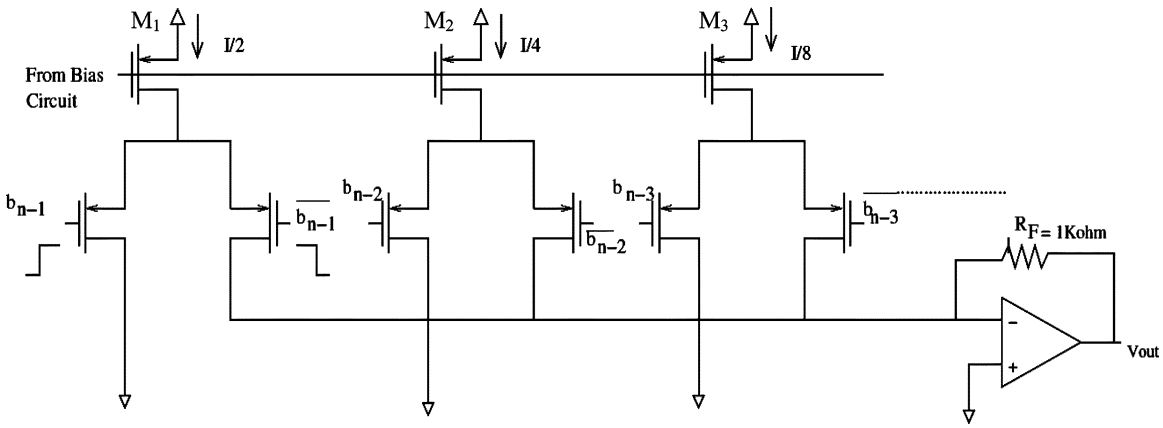

Fig. 13. Current steering DAC intended for high-speed applications. A six-bit DAC has been implemented using SPICE.

While doing so, it has been observed that the maximum stress on M_2 occurs when Vin^+ is at 0 V. So, keeping Vin^+ at 0 V and Vin^- at $V_{\mathrm{DD}}/2$, the variation in offset voltage (V_{OS}) is plotted in Fig. 12 as a function of ΔV_{th}. Fig. 12 (left axis) shows the variation of input referred offset voltage (V_{OS}) as a function of ΔV_{th} (of M_5, M_7, M_{10}, and M_{11}), while Fig. 12 (right axis) shows the difference between gate voltages of M_1 and M_2. The unequal stressing in M_1 and M_2 therefore must be taken in to account to effectively determine the circuit behavior due to NBTI. As can be seen from Fig. 12, the degradation becomes considerable when the op-amp circuit considered in Fig. 9 is used as a comparator. This is an important consideration to keep in mind since the same circuit behaves differently from the NBTI point of view when used for a different application.

D. Current Steering Digital-to-Analog Converter

The schematic diagram of a current steering digital to analog converter is shown in Fig. 13. This configuration of DAC is generally intended for high data rate applications. For biasing purposes, we have used the circuit shown in Fig. 5(c) (not shown in Fig. 13), which has been shown to have excellent stability against NBTI variations. The normalized output voltage of the DAC is given by (3).

$$V_n = \left(\frac{V_{\mathrm{out}}}{R_F I}\right) = \frac{\left(1+\frac{\Delta I}{I}\right)}{2^n}(D) \tag{3}$$

where ΔI is the change in biasing current, n the number of bits, and D the decimal equivalent of the i/p digital word. The maximum output error ΔV_{nmax} which occurs at $D = 2^n - 1$ is shown in (4) and the maximum allowable error (1/2 LSB) is as follows:

$$\Delta V_{n\,\max} = \left(1 - \frac{1}{2^n}\right)\left(\frac{\Delta I}{I}\right) \tag{4}$$

$$\frac{1}{2}LSB = \frac{1}{2^{n+1}}. \tag{5}$$

A six-bit DAC (of the configuration shown in Fig. 13) has been simulated and the transfer characteristics along with the error voltage for different ΔV_{th}'s are plotted as shown in Fig. 14. It can be observed from the figure that the maximum error voltage is almost reaching the allowed error of 1/2 LSB $(= 0.0078)$ for a digital input of 64 at a ΔV_{th} as low as 40 mV. Thus, variations in biasing currents due to NBTI resulted in a gain error for the DAC. However, mismatch between

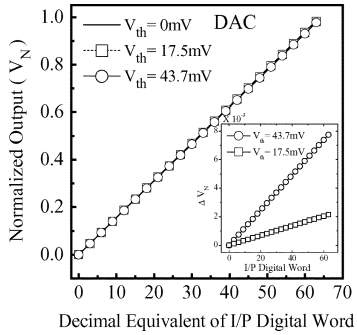

Fig. 14. Transfer characteristics of the six-bit DAC shown in Fig. 13. The inset shows the output error voltages for different threshold voltage variations. Degradation is identical in all the current mirrored pMOS devices.

current mirror paired devices $(M_1, M_2, M_3 \ldots)$ can cause nonlinear errors [11]. But, as all these devices undergo identical gate biasing, NBTI-induced mismatch is not considerable and also they degrade identically. Thus, for circuits like this DAC, NBTI induces gain errors rather than nonlinear errors.

V. Conclusion

A methodology to quantify the degradation at *circuit level* due to NBTI has been illustrated. Using this approach, current mirror circuits, op-amp, comparator, and a digital-to-analog converter are simulated for their NBTI reliability performance and their degradation is analyzed. It has been shown that the degradation in circuit performance is mainly dependent on its configuration and application rather than the absolute degradation at the device level. In circuits such as digital-to-analog converters, NBTI can pose a serious reliability concern as even a small variation in bias currents can cause significant gain errors. The general framework proposed in this work can also be extended for mapping different device-level reliability issues to the circuit performance degradation.

References

[1] Y. Yamamoto, K. Uwasawa, and T. Mogami, "Bias temperature instability in scaled p+ polysilicon gate p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 921–926, May 1999.

[2] N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai, and T. Horiuchi, "Impact for bias-temperature stability for direct tunneling ultrathin gate oxide on MOSFET scaling," in *VLSI Symp. Tech. Dig.*, 1999, pp. 73–74.

[3] C. H. Liu, M. T. Lee, C. Y. Lin, I. Chen, K. Schruefer, J. Brighten, N. Rovedo, T. B. Hook, M. V. Khare, S. F. Huang, C. Wann, T. C. Chen, and T. H. Ning, "Mechanism and process dependence of negative bias temperature instability (NBTI) for pMOSFET's with ultrathin gate dielectrics," in *IEDM Tech. Dig.*, 2001, pp. 861–864.
[4] A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriguez, S. John, and S. Krishnan, "NBTI impact on transistor and circuit: model, mechanism and scaling effects," in *IEDM Tech. Dig.*, 2003, pp. 349–352.
[5] Y.-H. Lee, N. Mielke, B. Sabi, S. Stadler, R. Nachman, and S. Hu, "Effect of pMOST bias-temperature instability on circuit reliability performance," in *IEDM Tech. Dig.*, 2003, pp. 353–356.
[6] D. Schroder and J. F. Bobcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, pp. 1–18, Jul. 2003.
[7] V. Reddy, J. Carulli, A. Krishnan, W. Bosch, and B. Burgess, "Impact of negative bias temperature instability on product parametric drift," in *Proc. Int. Test Conf.*, 2004, pp. 148–155.
[8] P. Chaparala and D. Brisbin, "Impact of NBTI and HCI on PMOSFET threshold voltage drift," *Microelectron. Reliab.*, vol. 45, pp. 13–18, 2005.
[9] R. Thewes, R. Brederlow, C. Schliinder, P. Wieczorek, A. Hesener, B. Ankele, P. Klein, S. Kessel, and W. Weber, "Device reliability in analog CMOS applications," in *IEDM Tech. Dig.*, 1999, pp. 81–84.
[10] R. Thewes, R. Brederlow, C. Schliinder, P. Wieczorek, B. Ankele, A. Hesener, I. Holz, S. Kessel, and W. Weber, "MOS transistor reliability under analog operations," *Microelectron. Reliab.*, vol. 40, pp. 1545–1554, 2000.
[11] M. Agostinelli, S. Lau, S. Pae, P. Marzolf, H. Muthali, and S. Jacobs, "PMOS NBTI-induced circuit mismatch in advanced technologies," in *Proc. Int. Reliability Physics Symp.*, 2004, pp. 273–282.
[12] P. Chaparala, D. Brisbin, and J. Shibley, "NBTI in dual gate oxide PMOSFETs," in *Proc. Int. Symp. Plasma and Process-Induced Damage*, 2003, pp. 138–141.
[13] Y. Nishida, H. Sayama, K. Ohta, H. Oda, M. Katayama, Y. Inoue, H. Morimoto, and M. Inuishi, "SoC CMOS technology for NBTI/CHC immune I/O and analog circuits implementing surface and buried channel structures," in *IEDM Tech. Dig.*, 2001, pp. 869–872.
[14] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MOS devices," *J. Appl. Phys.*, vol. 48, pp. 2004–2016, 1977.
[15] C. Blat, E. Nicollian, and E. Poindexter, "Mechanism of negative-bias-temperature instability," *J. Appl. Phys.*, vol. 69, no. 3, pp. 1712–1720, 1991.
[16] S. Ogawa and N. Shiono, "Generalized diffusion-reaction model for the low-field charge build up instability at the $Si-SiO_2$ interface," *Phys. Rev. B, COndens. Matter*, vol. 51, no. 7, pp. 4218–4230, 1995.
[17] S. Ogawa, M. Shimaya, and N. Shiono, "Interface-trap generation at ultrathin SiO_2 (4–6 nm)-Si interfaces during negative-bias temperature aging," *J. Appl. Phys.*, vol. 77, pp. 1137–1148, 1995.
[18] S. Mahapatra, P. B. Kumar, and M. A. Alam, "A new observation of enhanced bias temperature instability in thin gate oxide p-MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 196–202.
[19] S. Mahapatra and M. A. Alam, "A predictive reliability model for pMOS bias temperature degradation," in *IEDM Tech. Dig.*, 2002, pp. 505–509.
[20] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, "A comprehensive framework for predictive modeling of negative bias temperature instability," in *Proc. Int. Reliability Physics Symp.*, 2004, pp. 273–282.
[21] G. Chen, K. Y. Chuah, M. F. Li, D. S. H. Chan, C. H. Ang, J. Z. Zhcng, Y. Jin, and D. L. Kwong, "Dynamic NBTI of pMOS transistors and its impact on device lifetime," in *Proc. Int. Reliability Physics Symp.*, 2003, pp. 196–202.
[22] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for p-MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 345–348.
[23] S. Tsujikawa, T. Mine, K. Watanabe, Y. Shimamoto, R. Tsuchiya, K. Ohnishi, T. Onai, J. Yugami, and S. Kimura, "Negative bias temperature instability of pMOSFET's with ultrathin SiON gate dielectrics," in *Proc. Int Reliability Physics Symp.*, 2003, pp. 183–188.
[24] S. Rangan, N. Mielke, and E. Yeh, "Universal recovery behavior of negative bias temperature instability," in *IEDM Tech. Dig.*, 2003, pp. 341–344.
[25] C. Schlunder, R. Brederlow, B. Ankele, W. Gustin, K. Goser, and R. Thewes, "Effects of inhomogeneous negative bias temperature stress on p-channel MOSFET's of analog and RF circuits," *Microelectron. Reliab.*, vol. 45, pp. 39–46, 2005.
[26] N. K. Jha, P. S. Reddy, and V. R. Rao, "A new drain voltage enhanced NBTI degradation mechanism," in *Proc. Int. Reliability Physics Symp.*, 2005, pp. 524–528.
[27] M. Alam, J. Bude, and J. Ghetti, "A. Field acceleration for oxide breakdown-can an accurate anode hole injection model resolve the E versus 1/E controversy?," in *Proc Int Reliability Phys Symp*, 2000, pp. 21–26.
[28] *ISE TCAD Version 8.0 User's Manual*, 2002.
[29] J. M. Steininger, "Understanding wide-band MOS transistors," *IEEE Circuits Devices*, vol. 6, no. 3, pp. 26–31, May 1990.

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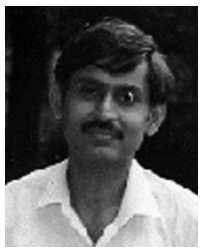

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