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Modelling, analysis, and acceleration of a printed circuit board fabrication process

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Abstract. Product design and fabrication constitute an important business activity in any manufacturing firm. Designing an optimized product fabrication process is an important problem in itself and is of significant practical and research interest. In this paper, we look into a printed circuit board (PCB) fabrication process and investigate ways in which the fabrication cycle time can be minimized. Single class queueing networks constitute the modelling framework for our study. The model developed in this paper and the analysis experiments carried out are based on extensive data collected on a PCB fabrication company located in Bangalore, India. This is a representative PCB fabrication company involving multiple, concurrent fabrication works with contention for human/technical resources. Our model seeks to capture faithfully the flow of the fabrication process in this company and such other organisations, using queueing networks. Using the model developed, we explore how the cycle times can be reduced using input control, load balancing, and variability reduction. The model presented is sufficiently generic and conceptual; its scope extends beyond that of a PCB fabrication organization.

Keywords. Queueing; manufacturing; modelling; cycle times.

1. Introduction

While manufacturing firms have been developing new products since the industrial revolution, the importance of designing and developing high quality new products has increased dramatically in recent years. The main forces driving the importance of product design and development are competition – internal and external to the company, changing customer needs, and changes in technology. These driving forces have created a competitive imperative for speed, efficiency, and high quality in the design and development process. This creates substantial pressure on engineering teams to develop better products and at the same time to develop them faster. It is also observed from various studies (Hopp

et al 1990; Milson *et al* 1992) that product life cycles are continuously becoming shorter, which has forced companies to reduce the product design and development lead time. At the same time, the effects of shorter lead times can be considered beneficial only if they can be achieved without undue sacrifices in other areas such as quality. Recent literature on lead time modelling of product design and development has revealed many techniques for faster development of new products (Millson *et al* 1992). These techniques are based on some generic approaches, which focus on the reduction of lead time. Companies follow one or a combination of these approaches to accelerate the product design and development cycle. However, these approaches can be applied only when the entire process is clearly understood, which is achieved through faithful modelling of the process.

Our objective in this paper is to model and analyse a typical industrial fabrication process and to investigate the methods to reduce fabrication cycle time. We specifically consider the PCB fabrication process. We apply queueing theory to model this process, and, using the model developed, we explore the improvement in fabrication cycle time using input control, load balancing, and variability control.

1.1 *Review of relevant work*

Considerable amount of research has been carried out in the past decade in the important areas of lead time modelling and lead time reduction in a manufacturing firm. For example, Hopp *et al* (1990) in their paper have explored the causes of excessive lead time and suggest practical, inexpensive strategies for reducing lead time. Their suggestions are based on a detailed study of six manufacturing companies and a survey of literature in the related area. Hopp & Spearman (1996) have listed several techniques (based on queueing principles) for compressing manufacturing lead times. Some of the techniques for lead-time reduction discussed by them, such as variability reduction, have been explored in our work in the current paper. Quick response manufacturing (QRM), presented by Suri *et al* (1995) and Suri (1998) is an important collection of techniques to compress process lead times in manufacturing firms. QRM principles include intelligent scheduling of bottleneck resources, product-oriented cellular organization, use of a judicious mix of push and pull control policies etc. It is argued that substantial improvement in lead time, of the order of 75%, in new product introduction, and 90% to fill orders for existing products can be achieved by using QRM techniques. Apart from reductions in lead times, when properly implemented, a QRM strategy also results in quality improvement and cost reductions.

Lead time reduction techniques have been popular in the context of the product design process and in new product development processes also. Millson *et al* (1992) present a survey of major approaches for accelerating new product development. They suggest a general set of techniques for reducing the development cycle time of new products, and classify these techniques into five basic categories. These are: (a) Simplify the process; (b) eliminate the delays; (c) eliminate steps; (d) speed up operations; and (e) make processes parallel. There are several books that have appeared in recent years, which focus on improving the product development process. In their book, Clark & Wheelwright (1993) discuss lead time reduction in a qualitative way with illustrative case studies. Krishnan *et al* (1995) in their study, have discussed a method of reducing product development lead time by overlapping development activities through the exchange of preliminary design information. In their approach, downstream development activities begin with

unfinalized upstream design information, and new design changes are incorporated in the subsequent iteration of development. Adler *et al* (1995, 1996) have analysed product development lead time in organizations that involve multiple, concurrent, non-unique projects, with shared resources, using single-class queueing network models. In fact, many of the techniques explored by us in the current paper, such as input control, process control, and load balancing, are suggested by these two papers. More recently, Narahari *et al* (1999) in their study have come up with lead-time models of product design and development processes using both single-class and multi-class queueing network models, and explored lead-time reduction using various lead-time reduction techniques. These techniques (Narahari *et al* 1999) have also inspired the current-work. Similar modelling and optimizing techniques are investigated for software product development by Nagaraju (1997).

Process models offer a systematic, well defined way of representing the structure of process. They record activities that are performed in the process with the inter-dependencies among activities. Lyons *et al* (1995), in their report, have explained key requirements, industry practices, and research questions that should drive new methods and computer tools for process modeling of the product realization.

1.2 *Queueing networks*

A queueing network is a collection of stations (or service facilities) arranged in such a way that the customers proceed from one station to another in order to fulfill their service requirements. Each station has an associated queue in which jobs may wait prior to receiving service. The stations are characterized by service rate and the queueing discipline. The service rate is the number of jobs departing from the station per unit time, and queueing discipline is the order in which arriving jobs receive service. A queueing network is said to be Open Queueing Network (OQN), if customers are permitted to enter or leave, whereas a network is said to be Closed Queueing Network (CQN), if the number of customers in the network remain same at all times. A queueing network may contain several classes of customers. Customers of a particular class have identical service requirement.

Queueing networks have been widely used in the modeling of manufacturing and production processes (Viswanadham & Narahari 1992; Hopp & Spearman 1996). A workpiece or a job in a factory floor goes through a sequence of operations in multiple machine centres, waiting in multiple queues during its journey in the production process. Queueing networks can capture very accurately the flow of jobs, contention for resources, and the waiting periods. Using these models, the manufacturing lead time can be computed and lead time reduction strategies can be experimented with. This motivates the use of queueing networks to model the flow of PCB jobs in a PCB fabrication facility.

1.3 *Analysis tools*

Two software packages are used to analyses the performance measures of PCB fabrication process considered. These software packages have been developed at the Department of Computer Science and Automation, Indian Institute of Science, Bangalore.

1.3a Open queueing network analyser: This tool analyses open Jackson queueing networks with multiserver stations (Viswanadham & Narahari 1992). The inputs to the package are (Kiran Kumar 1995):

- Number of stations in the network;
- number of servers at each station;
- external arrival rate of jobs at each station;
- service rate of each station;
- routing probabilities;
- squared coefficient variation (SCV) of arrival rate;
- SCV of service rate of each station.

The tool evaluates the utilization of each station, visit counts, waiting time, and number of jobs at each station, and total number of jobs and total wait time of the network.

1.3b Closed queueing network analyser: This tool uses the mean value analysis to evaluate the performance measures of the CQN. The input to the packages are (Kiran Kumar 1995):

- Number of stations in the network;
- number of jobs in the network;
- service rate of each station;
- routing probabilities.

The tool evaluates visit counts at each station, queue length, waiting time at each station and total waiting time of the network.

1.4 *Outline of the paper*

In §2 of this paper, we describe the PCB fabrication process as seen in our representative company, which we call as PCB-FAB. In §3, we present a model of this PCB fabrication process based on single class open queueing networks. In §4, we analyses the model developed, using software tools. With these analytical tools, we investigate the variation of the mean cycle time and the variance of cycle time with input rate, squared coefficient variation of interarrival time and the mean number of customers in the system. In §5, we present the practical implications of our study.

2. PCB fabrication process: An outline

Printed circuit boards are found virtually in all electronic equipments. They are also the most custom-designed part of any electronic equipment. PCBs provide mechanical support apart from functional electrical interconnection between components. A PCB is a dielectric substrate with metallic circuitry photo-chemically formed upon that substrate. Typically, there are two major types of board materials (dielectric substrates) that are used for the baseboard, fiberglass (glass-epoxy) and phenolic paper. The baseboard is also known as copper clad. There are three types of printed circuit boards available today. They are

(i) *Single sided boards*: Where the entire circuit is laid on one side of the board and there may or may not be holes on the board for mounting of components, or for interconnection of components.

(ii) *Double sided boards*: With the circuit on both sides of the board and electrical connection is established by drilling holes through the board and plating copper through the holes.

(iii) *Multilayer boards*: Two or more pieces of dielectric materials with circuitry formed upon them and are stacked up and bonded together. Electrical connections are established from one side to the other, and to the inner layer circuitry by drilled holes which are subsequently plated through with copper.

Printed circuit technology may be divided into three basic phases or stages: Engineering, photography and fabrication. The circuit diagram in the form of a schematic diagram is photo-plotted on a film which is one of the inputs for the fabrication process. The following paragraphs briefly describe the stages involved in the PCB fabrication process. Figure 1 shows the various stages in the PCB fabrication process.

2.1 *Photo film inspection*

The following documentations required for the fabrication process are collected from the customer, along with the sales order: schematic drawings, manufacturing specifications, circuit films, drilling details, and CNC drill data etc. Once these documentations are reviewed for their correctness, then contact films are developed from the circuit films. These contact films are used in fabrication process. If the documents are not suitable for fabrication, it is returned back to the customer.

2.2 *Panel cutting*

Copper clads with thin layer of copper on both sides are used for fabrication of double sided PCB. The standard thickness of copper layer is 18 and 35mm. This copper clad is cut into pieces. These pieces of copper clad are called as panels. Depending on the size of PCBs to be fabricated, a panel accommodate one or more than one PCB. Cutting these panels to the PCBs of the required size is done at the trimming stage of the process. On all the four sides of the panel, extra space is left which is required to hold the panel during different stages of fabrication process, without affecting the PCB area.

2.3 *Drilling holes*

Once the panel is cut, the next stage is the drilling of holes. Either CNC drilling or manual drilling is used for this purpose. It is observed from past data that 98.92% of the jobs are drilled on CNC drilling machine and only 1.08% of the jobs are drilled on optical drilling (manual). Manual drilling is only used in one or more of the following situations: (1) very low order quantities, (2) non-availability of drill data, and (3) number of holes on the PCB is too low for using the CNC drilling machine. The panels are pinned together in stacks from one to four high, depending on panel thickness. These are loaded onto the drilling machine. NC part program is loaded into the CNC drilling machine and all required holes are drilled at proper locations, with correct drill size. Latest CNC drilling machines are equipped with automatic tool changer which will automatically change drill bits when the hole size changes. Some CNC drilling machines are also equipped with multiple spindle, so that simultaneously multiple stacks of panels can be drilled. Once all the holes are drilled, the panel is cleaned and deburred.

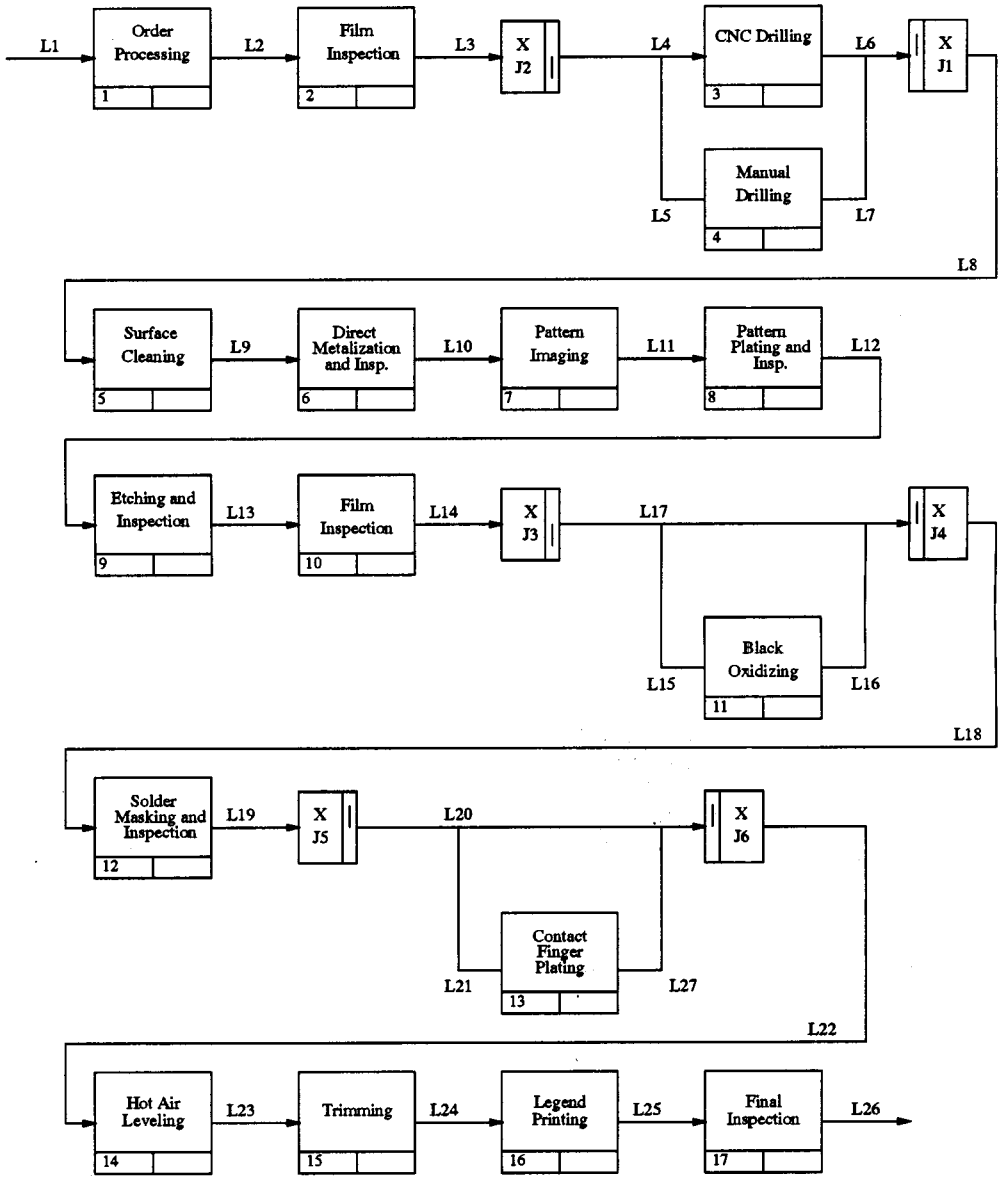

Figure 1. Various steps in the PCB fabrication process.

2.4 *Electro-less copper plating*

Once the panel is deburred and inspected, then it goes to the next stage, that is, electro-less copper plating. The sole purpose of electro-less copper plating is to metallize the wall of drilled holes. This hole metallization (1) provides an electrical connection between the two sides of the board, and (2) serves as a metal substrate upon which subsequent copper may be deposited electrolytically. This connectivity is done by peridium coating

on the inner side of holes by passing each panel through a series of electrolyte baths. After this is done the panel is cleaned and dried.

2.5 *Pattern imaging*

After the holes have been plated, the circuit pattern is imaged on to each of the panels. The image defines the circuit for plating and etching purposes. Negative circuit film is used for this purpose. Both sides of the panel are coated with a thin layer of dry film photo resist. The circuit film is laid on one side of the drilled panel and exposed to ultraviolet light. Except the circuit area, all the other area on the panel is polymerized and hence becomes hard. This is repeated for the other side. The unexposed photo resist is washed away during development, to leave the circuit pattern. This process is carried out for each panel.

2.6 *Pattern plating*

In this stage of the fabrication process, the thickness of copper tracks on the panel is increased by 20 – 30 mm. Over the copper tracks, tin-lead plating is done, which (1) protects the conductive copper from oxidation thereby preserving solderability, and (2) acts as etch resist for the subsequent etching stage to follow.

2.7 *Etching and tin-stripping*

Once the pattern plating is done, the dry film photo resist is stripped by a solvent. This bares the unwanted copper foil which is etched away to leave the plated circuit. Copper foil is etched by spraying the etchant to both sides of the panel as it moves on a conveyor.

2.8 *Solder masking*

Solder mask is an epoxy barrier applied to one or more sides of the panels. It prevents solder bridges from forming during the wave soldering operation performed by the board user. It also reduces the ability of molten solder to adhere to the board's surface, and acts as a barrier which prevents damage to the circuitry due to scratches. The solder mask is typically applied by screen printing using solder mask film which enables the entire board surface to be covered, except for the holes, pads and contact fingers.

2.9 *Contact finger plating*

Contact finger plating is the next operation (optional) in the fabrication of PCBs. Contact fingers are the rows of tabs along one or more edges of the boards. These tabs fit into connectors in the electronic equipment in which the PCB is used. They must be durable and resistant to tarnishing and oxidation. Over the bare copper tracks, plating is done first with nickel, then with gold. Nickel serves as a wear-resistant barrier between the copper and gold and gold is used on the top because of its excellent conductivity and resistance to oxidation.

2.10 *Hot air leveling*

During this stage of the fabrication process, the panels are dipped in solder bath, so that all PTHs and solder points are covered with tin-lead plating. These panels are passed through a conveyor, while hot air is blown from one side of the panel, so that all the tin-lead covered holes are cleared.

2.11 *Trimming*

During this stage of the process, the panels are cut to the required size of individual PCB. Printed circuit boards contain holes which are plated through and some which are not to have any plating in them at all. Since the electro-less copper process will deposit copper inside drilled holes, a second drilling step is needed. These holes are mainly used for mounting the components and fixing the connectors etc.

2.12 *Legend printing*

The legend or nomenclature, is screen-printed onto PCBs to identify the components, for assembling and testing purposes. This screen-printing operation is performed using legend print film supplied by the customer. Since legend is permanent, once it is dried, legend-printed panels must also be checked for legibility and completeness of the printed image.

2.13 *Inspection*

Inspection is done at various stages of the fabrication process. If the panel is accepted at that stage, it is passed on to the next stage. Otherwise it goes back to rework, to the same stage of operation. In some cases, when the panel is beyond rework, it is rejected.

3. A queueing network model of PCB fabrication

Figures 2 and 3 show the two parts of a queueing network model of the printed circuit board fabrication process. The description of service rendered to the job at each stage of the process is explained in §2.

A new job enters the system at station number 1, that is, O.Proc (order processing) and successfully completed jobs exit the system from station Del. (delivery of PCBs). Each job undergoes a sequence of operations in the manner shown in figures 2 & 3. For example, after successfully finishing processing at P.cut (station 3), a job is routed to either a CNC drilling station (with probability 0.9892) or a manual drilling station (with probability 0.0108). These probabilities are chosen based on past data available (which showed that 98.92% of the jobs underwent CNC drilling). A job can visit a station several times due to rework. The probability of returning to the previous stage after completing service at a particular station is shown for all appropriate feedback possibilities. For example, after inspection at station number 11, a job will come back to station number 10 (Copper and Tin Plating) for rework and the probability of this feedback is 0.155. This means that with a probability of 0.845, the job will go to the

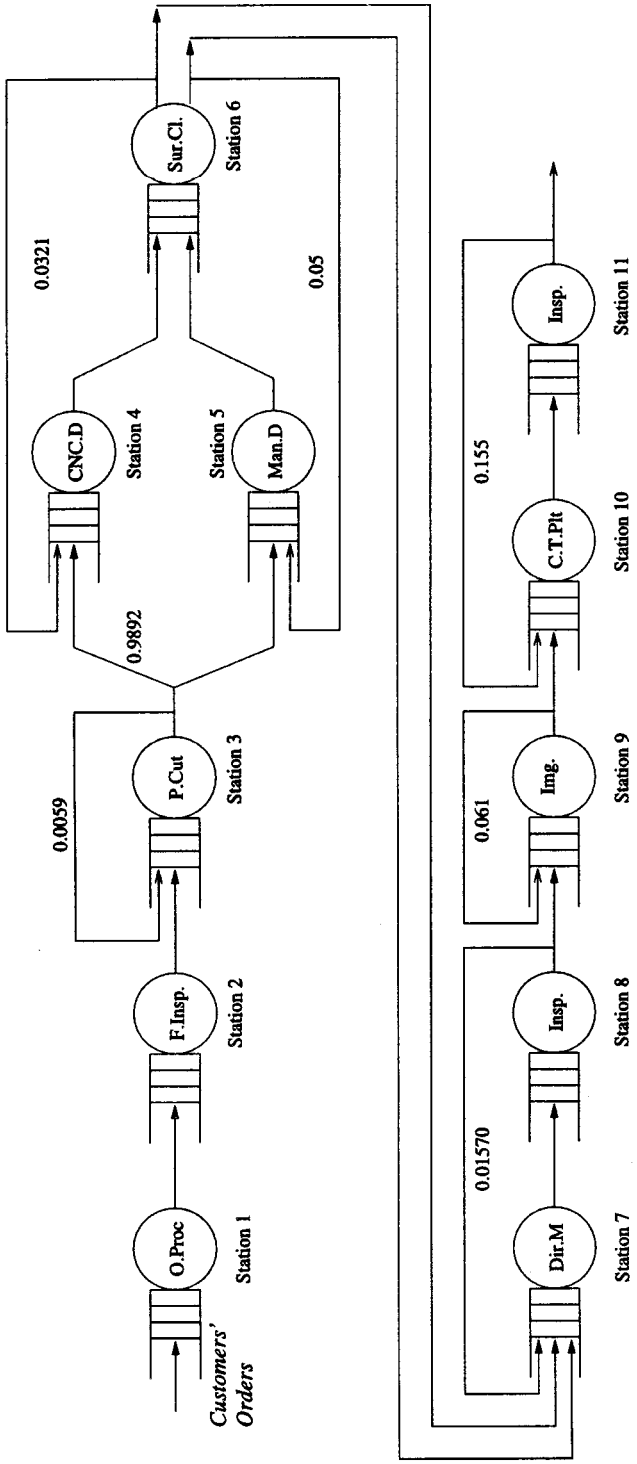

Figure 2. Part 1 of a queueing network model for the PCB fabrication process.

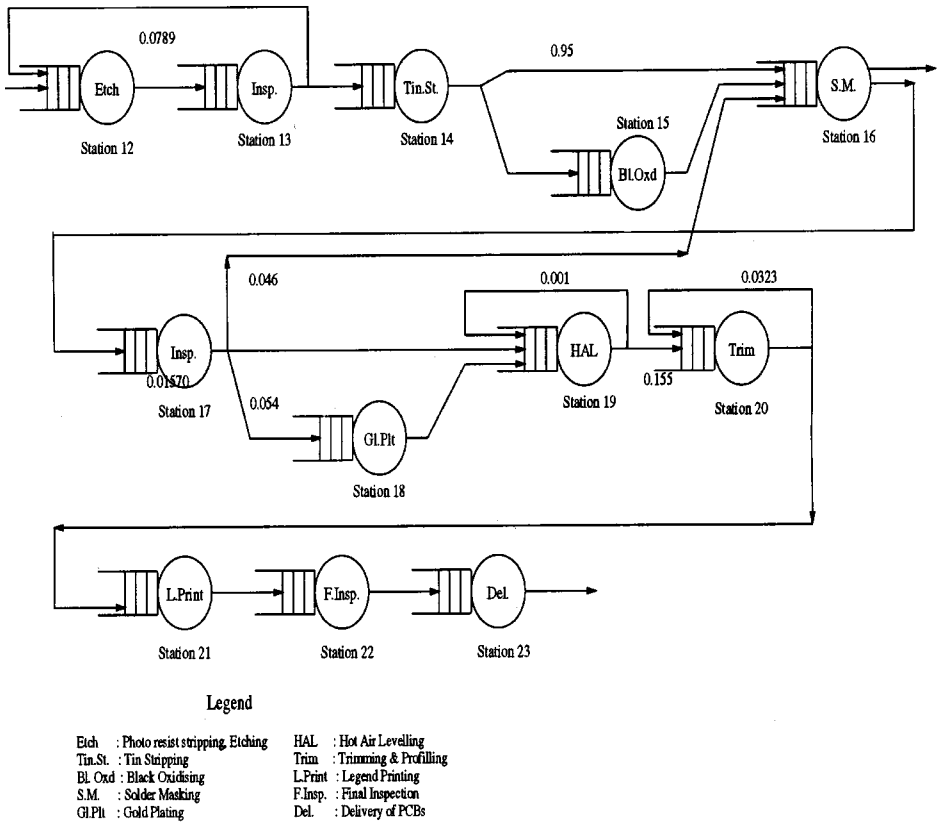

Figure 3. Part 2 of a queueing network model for the PCB fabrication process.

next stage, that is, etching. These feedbacks are represented by backward arrows in the figure, while the forward arrows indicate that the process is successfully completed at that station. The number near the feedback arrows indicates the probability of failure at that station, and hence the probability of rework. Since most of the stages of fabrication process involve chemical action, we have made the reasonable assumption that the service time distribution at a station for a job visiting the station for the first time is the same as that of the fed-back jobs. The routing probability is independent of the previous history of the job.

We have obtained the data pertaining to inter-arrival time between successive new jobs, the service times at various stations, the feedback probabilities either by interviewing the company personnel or from their record book. For our experiment we have considered the fabrication of PCBs with a batch size of 100. In this PCB-FAB, most of the processing stages do batch processing with a batch size of 100. That is, there is a setup time for each batch and then 100 PCBs are processed (either sequentially or in smaller batches) until 100 PCBs are processed and then there is a new setup for the next batch of 100 PCBs. The processing time at each stage, therefore, corresponds to a single setup time (for the entire batch of 100) plus the total execution time for 100 PCBs. The mean service rate at each station is calculated according to the data we obtained from the company and are shown in table 1. We have considered the unit of time as one day.

Table 1. Service rates at different stations for the base model of PCB fabrication process.

S. No.	Station name	Working hours/day	Mean service time (min)	Mean service time (days)	Service rate
1	Order processing	8.0	120	0.2500	4.0000
2	Film inspection	8.0	35	0.0729	13.7143
3	Panel cutting	8.0	50	0.1042	9.6000
4	CNC cutting	24.0	500	0.3472	2.8800
5	Manual drilling	24.0	1080	0.7500	1.3333
6	Surface cleaning	24.0	200	0.1389	7.2000
7	Direct metallization	24.0	120	0.0833	12.0000
8	Inspection	8.0	100	0.2083	4.8000
9	Imaging	24.0	350	0.2431	4.1143
10	Copper and tin plating	24.0	300	0.2083	4.8000
11	Inspection	8.0	100	0.2083	4.8000
12	Etching	24.0	400	0.2778	3.6000
13	Inspection	8.0	100	0.2083	4.8000
14	Tin stripping	24.0	300	0.2083	4.8000
15	Black oxidising	24.0	120	0.0833	12.0000
16	Solder masking	24.0	235	0.1632	6.1277
17	Inspection	8.0	120	0.2500	4.0000
18	Gold plating	24.0	240	0.1667	6.0000
19	Hot air levelling	24.0	200	0.1389	7.2000
20	Trimming	24.0	200	0.1389	7.2000
21	Legend printing	24.0	100	0.0694	14,4000
22	Final inspection	8.0	15	0.0313	32.0000

The mean service times tabulated in table 1 above are considered, for a batch size of 100 double-sided PCB fabrication, with two PCBs per panel, and $2000-2500$ holes each.

The QN model is thus described by the following parameters: Number of nodes, mean and variance of inter-arrival time between successive new jobs, mean and variance of service time distribution at each station, routing matrix, and the scheduling policy to be followed at each station. We assume that a non-preemptive FCFS policy is followed at each station. We also assume that the buffers at all the stations have infinite capacity.

4. Fabrication cycle time reduction

The main purpose of our study is to evaluate the performance of the model of figures 2 and 3, and explore several opportunities for cycle time reduction, as cycle time is the most important performance measure. Other performance measures such as mean number of jobs in progress, utilization of resources can also be computed. Since the model is a single class open-queueing network with single-server station, Markovian routing, general inter-arrival times, and general service times, we have used the software package developed at the Indian Institute of Science (Kiran Kumar 1995). The performance measures are computed using analytical formulae.

Based on the data collected at the company PCB-FAB, we first created a base model for which we chose inter-arrival time of 2 jobs/day. With this data, the base model gives a mean cycle time of 7.075 days, if the service times are assumed to be exponentially distributed with mean service time as in table 1. Table 2 shows the variations of mean cycle time for different inter arrival times (IATs). Cycle time increases nonlinearly with

Table 2. Mean cycle time for various input arrival processes.

Mean IAT (days) for batch of 100	Mean cycle time in days		
	Poisson arrivals	Uniform arrivals	Deterministic arrivals
0.901	4.838152	4.344657	4.282018
0.571	6.211016	5.606141	5.521283
0.500	7.075244	6.420974	6.326138
0.466	7.761732	7.058958	6.955073
0.417	9.612223	8.732203	8.597173
0.391	12.061462	10.864682	10.675641
0.376	15.805556	14.025449	13.737866
0.367	22.378527	19.469528	18.991804
0.363	34.725552	29.608326	28.758997
0.360	61.668919	51.664593	49.993061
0.359	119.294205	98.794846	95.357758
0.358	253.370178	208.427353	200.878296
0.3578	485.777588	398.455322	383.776978

the input arrival rate. This is because of the congestion of many jobs at bottleneck stations like CNC drilling and etching.

4.1 *Cycle time reduction through input control*

Since waiting times are positively correlated with the fluctuation in the arrival of incoming jobs, deterministic arrivals provide better cycle time. Table 2 shows the effect of input control on mean cycle time. The first column corresponds to the mean inter-arrival time for a batch of 100 PCBs, measured in days. In our base model, we have considered Poisson arrival distribution (where SCV of arrival is 1.0). The table shows that, if we reduce the fluctuation in arrival process, we can achieve a reduction in cycle time. We reduced the SCV of arrival rate from 1.0 (exponential arrival rate) to 0.144 (uniform arrival rate) to 0 (deterministic arrival rate). As the inter-arrival times become less variable, there is found to be considerable reduction in mean cycle times. The practical implication of this is that the PCB-FAB manager ought to schedule the arrival of raw materials and other items required to start fabrication in a careful way, so as to arrive as "deterministically" as possible. This in turn calls for effective communication and co-ordination with all vendors who supply the items that are required by the PCB-FAB.

The second method of reducing mean cycle time by controlling fluctuation in arrival of jobs is by allowing new job to enter the system only when a job in the system comes out of the system after finishing its entire processing. This ensures a constant population of jobs in the system. This type of system is modelled as a closed queueing network (CQN). The CQN improves the cycle time performance by eliminating the variability due to uncontrolled arrivals of job which are responsible for poor performance of OQN. Table 3 shows the effect of operating the system in fixed population mode. The routing probabilities are as in figure 1 and the mean service times are as in table 1. The first column gives the current population of the network in CQN mode; the second column gives the corresponding mean cycle time; the third column gives the mean inter-arrival time that is consequent on having the corresponding population in the closed network; the fourth column provides the corresponding throughput rate of jobs completed per day;

Table 3. Cycle time reduction through input control.

Population for closed model	Mean cycle time (days)	Associated mean IAT (days)	Throughput rate (per day)	Mean cycle time for open models (days)
5	4.504	0.901	1.110	4.838
10	5.710	0.571	1.751	6.211
13	6.469	0.500	2.0	7.075
15	6.990	0.466	2.146	7.762
20	8.343	0.417	2.397	9.612
25	9.772	0.391	2.558	12.061
30	11.279	0.376	2.660	15.806
35	11.286	0.367	2.722	22.379
40	14.507	0.363	2.757	34.726
45	16.206	0.360	2.777	61.669
50	17.941	0.359	2.787	119.294
55	19.700	0.358	2.792	253.370
60	21.473	0.3578	2.794	485.778

and the fifth column gives the mean cycle time of the same network operated in the open queueing network mode, to get the same throughput. From the table it is clear that the mean cycle time is reduced drastically if one operates the system in closed mode to get the same throughput. For example, for the population of 30, the mean cycle time is 11.279 days which corresponds to the throughput rate of 2.66 jobs/day. To achieve the same throughput rate in the open queueing network requires 15.806 days.

Note that the fixed population inside the network includes jobs that need reworking. The implication of having to maintain a fixed number of jobs inside the network is that we should schedule arrivals of raw materials for a new job to synchronise with the completion of processing of a job in the network. This again calls for smart co-ordination with vendors and intelligent order management.

4.2 *Cycle time reduction through process control*

We have seen in §4.1 above, that the mean cycle time can be reduced by controlling the variation in arrival rate of new jobs. Hence, the next logical move to reduce the mean cycle time is to control the variation in service time of individual station. This we call as process control. Table 4 shows effect of process control on mean cycle time. First three columns of the table show mean cycle time and mean number of jobs currently being serviced in the system, for various inter-arrival rates. It is assumed that arrival rate and service rates are exponential. The mean service time is taken from table 1 and the routing probabilities are as shown in figure 1. The next two columns correspond to mean cycle time and mean number of jobs for the same system, but with uniform distribution of service time. That is, the mean service time as shown in table 1, with SCV of 0.144. The last two columns give the mean cycle time and mean number of jobs currently being serviced for the same system, but with deterministic distribution of service times.

It is very clearly seen from the table that the reduction in mean cycle time can be achieved by controlling variation in service time, which implies controlling the process involved in the service station. This calls for effective use of best practice techniques such as statistical process control and such other variability reduction techniques.

Table 4. Mean cycle time with different service time variabilities.

Exponential service times			Uniform service times		Deterministic service times	
IAT (days)	Mean cycle time	Mean nos. of jobs	Mean cycle time	Mean nos. of jobs	Mean cycle time	Mean nos. of jobs
0.901	4.838	5.370	4.166	4.624	4.068	4.515
0.571	6.211	10.875	4.570	8.002	4.322	7.568
0.500	7.075	14.150	4.799	9.599	4.452	8.904
0.466	7.762	16.657	4.985	10.698	4.557	9.780
0.417	9.612	23.041	5.510	13.207	4.868	11.668
0.391	12.061	30.853	6.262	16.017	5.340	13.660
0.376	15.806	42.043	7.485	19.910	6.144	16.343
0.367	22.379	60.914	9.713	26.434	7.645	20.808
0.363	34.726	95.736	13.966	38.504	10.537	29.052
0.360	61.669	171.255	23.298	64.699	16.908	46.954
0.359	119.294	332.473	43.290	120.650	30.570	85.198
0.358	253.370	707.409	89.823	250.787	62.377	174.156
0.3578	485.778	1357.26	170.491	476.354	117.519	328.347

4.3 *Cycle time reduction through load balancing*

The mean cycle time for various input arrival rates is already shown in table 3. The same table is repeated in table 5, with additional columns for resource utilization of station 4 and station 12. It is clear from table 5 that station 4 and station 12 are bottleneck stations. The cycle time can be reduced drastically if additional resources are provided to stations 4 and 12. We take only one case, where we consider only station 4. Since station 4 is a drilling machine, adding one more machine to the facility is not a cost effective solution. Hence the alternate is to subcontract some of the jobs which enter station 4. We assume that 5% of jobs which enter station 4 for the first time are subcontracted outside, with the assumption that the service time for this 5% of job is the same as that of other jobs.

Table 5. Resource utilization of bottleneck stations.

Mean IAT	Mean cycle	Resource utilization of	
(days)	time (days)	Station 4	Station 12
0.901	4.838	0.3970	0.3348
0.571	6.211	0.6262	0.5281
0.500	7.075	0.7153	0.6032
0.466	7.762	0.7675	0.6472
0.417	9.612	0.8573	0.7229
0.391	12.061	0.9148	0.7715
0.376	15.806	0.9513	0.8022
0.367	22.379	0.9735	0.8209
0.363	34.726	0.9860	0.8315
0.360	61.669	0.9932	0.8375
0.359	119.294	0.9967	0.8405
0.358	253.370	0.9985	0.8421
0.3578	485.778	0.9992	0.8427

Table 6. Cycle time reduction through load balancing.

	Before load balancing		After load balancing		After load balancing	
Mean IAT (days)	Cycle time (days)	Resource utilization station 4	Cycle time (exponential service time)	Resource utilization station 4	Cycle time (uniform service time)	Cycle time (det. service time)
0.901	4.838	0.3970	4.550	0.3771	3.995	3.869
0.571	6.211	0.6262	5.721	0.5949	4.311	4.100
0.500	7.075	0.7153	6.420	0.6795	4.502	4.210
0.466	7.762	0.7675	6.950	0.7291	4.640	4.287
0.417	9.612	0.8573	8.238	0.8144	4.993	4.490
0.391	12.061	0.9148	9.588	0.8691	5.380	4.722
0.376	15.806	0.9513	10.978	0.9038	5.794	4.980
0.367	22.379	0.9735	12.265	0.9248	6.195	5.234
0.363	34.726	0.9860	13.302	0.9367	6.521	5.444
0.360	61.669	0.9932	14.061	0.9435	6.761	5.600
0.359	119.294	0.9967	14.505	0.9469	6.902	5.692
0.358	253.370	0.9985	14.746	0.9486	6.679	5.742
0.3578	485.778	0.9992	14.846	0.9493	7.011	5.763

Table 6 shows effect of load balancing on mean cycle time. Column 2 gives mean cycle time for the base model; column 3 is the resource utilization of station 4; column 4 gives mean cycle time with only 0.93974 of jobs from station 3 entering station 4 which is equivalent to adding additional resource to station 4. Column 5 shows utilization of station 4 after load balancing. From this table it is very clear that even 5% less load on station 4 drastically reduces the cycle time of the system. Further reduction in cycle time is obtained by process control explained earlier, on the load balanced system.

5. Practical implications of the results

Experiments conducted on the queueing network model of the PCB fabrication process to reduce the fabrication cycle time reveal the following insights. By controlling the input arrival rate of new jobs, 25% decrease in cycle time can be achieved, for a commonly observed input arrival rate of 2.5 jobs/day. This result shows that, if the variability in inter-arrival times of new jobs is minimized, the mean fabrication cycle time reduces. The message here is, accept a new order only when a job exits from the process, after completion of entire processing, thereby insuring constant population within the system. Certain amount of risk is involved here, in the sense that, one may have to reject some new orders when the system is full with its predefined number of job population, and sometimes getting a new order is difficult when a job is required to be inducted into the system. A practical way of looking at this is to intelligently schedule in-bound raw materials, chemicals, and boards from upstream vendors in such a way as to synchronize as far as possible with the departure of finished lots from the system. This calls for effective communication, constant interaction, and synergistic co-ordination with suppliers and customers.

If a well-laid out process is maintained, and followed at each station (thereby reducing the variability in service time) the overall cycle time can drop by significant amounts. We have seen that the majority of stations in the PCB fabrication process operations

are chemical in nature. Here the variability in processing time is very low and accurate processing times are insured by well-laid down procedures. Statistical process control techniques are also useful here. The variability in service times of other human-related activities like inspection, pattern imaging, and panel cutting, will also have to be reduced to compress the cycle time. This calls for appropriate measures by the management.

For an inter-arrival time of 2.5 orders/day, the cycle time reduces to 75%, if 5% of drilling jobs are subcontracted outside, thereby reducing the queueing time at the drilling station. The PCB-FAB company has already realized that CNC drilling is a bottleneck stage and the company has indeed been subcontracting a certain number of their drilling jobs to external partners.

Considering the result of the work carried out, there is enough scope for further research in the following areas. In our PCB fabrication process, we have assumed only double-sided PCB, which is the most commonly used PCB type. But fabrication of single sided PCB is also being done in the same company. Thus for accurate modelling of the PCB fabrication company PCB-FAB, it is necessary to model the fabrication process as a multi-class queueing network model. In this study, we have considered mean and variance of fabrication cycle time as our primary performance measures. The experiments carried out have only concentrated on improving cycle time performance. Other performance measures like work-in-process, throughput, and resource utilization have strong correlation to cycle time and therefore have not been explicitly considered. There are, however, other performance metrics which are important and therefore need to be looked into, such as: cost, quality, and reliability.

We have developed, analysed, and attempted to optimise the PCB fabrication process. This model is sufficiently generic and conceptual. Its scope extends beyond the PCB fabrication process. Similar modelling techniques can be used for modelling fabrication of any other product.

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