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A High Performance Three-Phase Telecom Supply Incorporating a HF Switched Mode Rectifier with a Phase Shifted PWM Controller

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Abstract

Telecom supplies need to conform to low Total Harmonic Distortion (THD) and high Power Factor (PF) as per IEC 61000-3-2 and IEEE 519-1992 standards. These high rating power supplies use a three phase utility in which low THD and high PF are realized via various passive and active wave shaping schemes. In this paper, a new design for three phase telecom power supplies is presented with circuit parameter values optimized for high performance in terms of a low THD, high PF, low ripple and high line and load regulation using a suitable combination of various strategies. The performance of the power supply is validated by extensive simulations.

Key Words: High Power Telecom Supply, Low THD, Phase Shifted PWM, Three Phase Switched Mode Rectifier, Unity Power Factor

I. INTRODUCTION

The increased use of telecom systems have led to increased harmonic content being injected into the utility and a low power factor. Both of these are caused by the non linear load behavior of [1] conventional diode rectifiers. High THD (Total Harmonic Distortion) violates EMI while a low PF (Power Factor) [1] is undesirable in electrical utilities. Telecom supplies now have to conform to low THD and high PF as per IEC 61000-3-2 and IEEE 519-1992 standards [1]. Low power (< 2 kW) supplies, usually employ single phase systems, while for high power (2 to 15 kW) systems employ three phase systems [1]–[10].

Single phase systems invariably use active Power Factor Correction (PFC) schemes, in which by active switching and control (Switched Mode Rectifiers SMR) of the line current, the current is made to follow a sinusoidal reference (usually the mains refernce waveform) so that it mimics the line voltage. This acheives unity PF and reduces THD to low levels. Most of such schemes require detection of the line current so that it may be incorporated into the feedback loop. Converters operating at a high frequency provide the benefits of galvanic isolation, a smaller size transformer and filter components. Single phase systems with a P $<$ 1kW have been reported which need line current detection [2], and which do not need current detection [3]. By the incorporation of a suitable PI (Proportional and Integral) voltage controller scheme, good output voltage regulation has been reported in [4] and [5]. A single phase circuit with a phase shifted PWM with unity PF and a low THD in the context of a UPS has been reported in [6].

For higher power, three phase utility based supplies are used in most applications. Three phase systems offer six pulse rectifications that inherently have a low THD and high PF. In these systems, both the passive and active wave shaping schemes are used for improving power quality at the ac mains. Passive schemes are used for low power low cost applications that avoid costly and complex active circuitry and for very high power applications where it is difficult for active control components to meet the high ratings. The intermediate power range uses both passive and active schemes.

Among the three phase systems using passive schemes, the use of multi-pulse (12-18 pulse or higher) rectifiers [7] offers an inherent low THD and high PF. An 18 pulse converter using a passive scheme, having a PI voltage controller [9] for good line and load regulation has been reported for a 12 kW supply. Active control schemes have been reported [2]–[10] where each individual phase has active control corresponding to single phase systems schemes. They offer all the advantages mentioned for single phase systems with a reduced THD and near unity PF due to the inherent multi-pulse feature. Additionally, by connecting the output secondary windings of boost dc-dc converters in series, the currents in the three

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phases are equalized leading to balanced three phase currents.

In this paper a new design for a three phase ac mains fed supply for a 60 Vdc and up to 300 A load is presented with circuit parameter values optimized for operation at high power (up to 18 kW) from a three phase utility, using a combination of several techniques. The individual phases use a PS-PWM (phase shifted - pulse width modulation) SMR (switched mode rectifier) [6] scheme that yields a very low THD (<4%) and near unity PF in the line currents of three phases. The series connection of converter secondary windings yields balanced three phase currents and galvanic isolation with the use of a light high frequency transformer, as in [9] and it provides 6 pulse rectification. Both of these together result in a smaller filter capacitor. A common PI controller at the output provides excellent line and load regulation. The design and operation of the proposed supply is validated by extensive simulations in MATLAB.

II. BASIC WORKING OF A SMR PS-PWM CIRCUIT

The circuit shown in Fig. 1 uses a diode rectifier at the AC mains, followed by a switched mode converter. It is supplied a rectified voltage V_R and draws a current I_R from the mains as per the switching scheme of the switches, and so it is called a Switched Mode Rectifier (SMR).

The input voltage V_R to the boost converter is a diode bridge rectified voltage from the mains voltage V_L, feeding a series inductor L_1. This is followed by a dc-dc converter circuit feeding a HF transformer primary winding. The capacitor C_1 is not for reducing the ripple in V_R rather, it reduces the harmonic reverse feed into the mains feeder lines, and so it is quite a small value. The converter switches T1, T2, T3 and T4 are suitably paralleled by free wheeling diodes (D_1 through D_4). The switches in one mode called the "transfer mode" of operation take the rectified mains voltage at its input and creates an alternating voltage on the converter primary winding, where the induced voltage in the secondary winding is full-wave rectified and supplied to the load R and duly paralleled by the filter capacitor C_2 for reducing voltage ripple. In this mode, the value of inductor current I_R reduces as the energy stored in the inductor is transferred to the load. In another mode, called the "storing mode," the primary winding is shorted by the switches storing the energy in the inductor, so that I_R increases. By adjusting the timings of the "storing mode" and "transfer mode" the current I_R can be shaped to be a sinusoidal waveform.

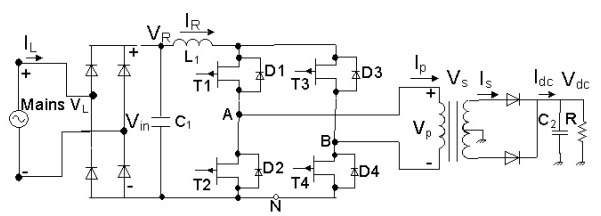


Fig. 1. Current Fed Boost Converter.

A. Energy Transfer Mode

In the "transfer mode" when the switches in cross locations i.e. T1 and T4 are ON (T1 = T4 = logic 1) and the other two cross switches T2 and T3 are OFF (T2 = T3 = logic 0), a polarity with top +ve in the primary winding as shown in Fig.2(c) is created. This transfer cycle is immediately succeeded by a "storing mode" cycle to be described in the next section. In the succeeding cycle, the switches T2 and T3 are ON while T1 and T4 are OFF to create a reverse polarity across the primary winding as shown in Fig. 2(e). The alternating voltage on the primary winding is "stepped down" in the secondary winding and full-wave rectified in the secondary winding circuit. In the transfer mode, voltage is induced in the secondary winding and the current flows in the secondary winding circuit feeding a current to the load R. This mode is called the "transfer mode," meaning that the energy is transferred from the primary winding to the secondary winding circuit. The energy is transferred from the inductor L_1 to R, so that the inductor current I_R reduces to a lower value.

The energy transferred to the load depends on the ON period of the cross switches when compared to the full cycle period. The ON period of 'T1 & T4' or 'T2 & T3' given by the "logic high" duration of T = T1.T4 + T2.T3 and is called the "transfer period" in the energy transfer mode. This period is variable and it is adjusted in the control scheme dynamically by comparing the reference and sensed dc voltages to offer good line and load regulation.

B. Energy Storing Mode

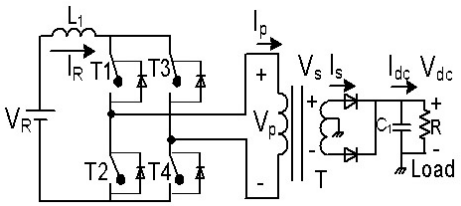
In this mode, in one cycle, the pair of switches in series say T1 & T2 in one path are turned ON while the corresponding pair of switches in the second path (T3 & T4) are kept OFF as shown in Fig. 2(b). In another cycle, T3 & T4 are ON while T1 & T2 are OFF as in Fig. 2(d). In this mode, the primary winding of the transformer is shorted by the switches, so that no energy is transferred to the secondary winding but instead the circuit in this mode allows the current I_R to build in the inductor L_1 and thereby increases energy stored in the inductor. Therefore, this mode is called the "storing mode." Its duration is given by the "logic high" period of T2.T3 + T1.T2 which is the complement of T.

C. Timing Sequence of Storing and Transfer Modes

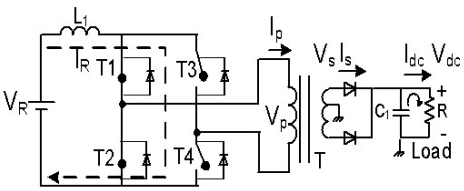
The gating scheme of the converter switches is such that the energy "storing" and "transfer" modes are activated alternately. The time period of the control pulses is kept constant. Part of the time period the inductor is "storing" energy while in the remaining part of the period the energy is transferred to the load. This cycle of alternating storing and transfer modes is shown in Fig.2 (b) through (e). The flow of the current is illustrated by dotted lines.

D. PWM Signal Generation Scheme

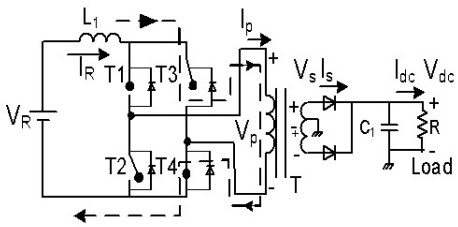
The circuit for generation of a control signal $V_{control}$ for PWM is shown in Fig. 3. The error V_e between the reference dc voltage V_{set} and the sensed dc voltage V_{dc} is subjected



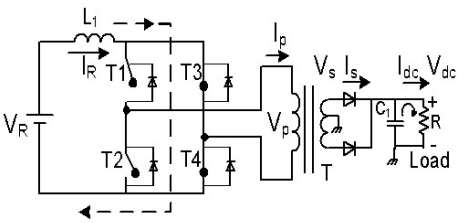
(a) Converter Schematic



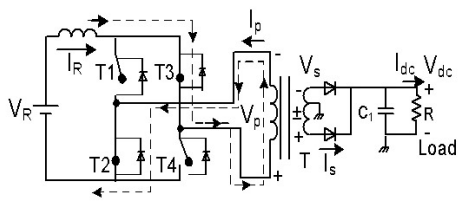
(b) Storing Mode(T1, T2-ON)



(c) Transfer Mode(T1, T4-ON)



(d) Storing Mode(T4, T3-ON)



(e) Transfer Mode(T3, T2-ON)

Fig. 2. Converter using PS-PWM Control Scheme.

to a proportional and integral (PI) controller as shown in Fig. 3. This is multiplied by the reference ac voltage V_{ac} ref (mains) voltage sampled from the line voltage so that the "total reference" signal contains the shape information of the mains voltage, and the output dc amplitude information from the PI controller signal. The sampled line current I_L is then compared with the "total reference" and the net error signal between the two is amplified and constitutes the control signal $V_{control}$ that is then compared with a high frequency triangular wave to generate the PWM waveform P.

In the positive cycle of the current if:

$$V_{control} > V_{tri} : \text{then } P = 1 \quad (1)$$

$$V_{control} < V_{tri} : \text{then } P = 0. \quad (2)$$

Similarly, in negative cycle of the current if:

$$V_{control} < V_{tri} : \text{then } P = 1 \quad (3)$$

$$V_{control} > V_{tri} : \text{then } P = 0. \quad (4)$$

E. Effects of the Energy Store and Transfer Mode Timings on the Rectifier Current Wave Shape and Output dc Voltage

It can be seen form Fig. 4 that if the PWM P waveform "high" period is large, then the "storing mode" lasts longer than the "transfer time," so that the rectifier current I_R increases in magnitude. For a smaller "high" time of P, the storing time is less than the transfer time so that the inductor current will be reduced. For equal times of energy storing and energy transfer, the rectifier current will be constant. Thus by measuring the error between the line voltage normalized shape and the sensed rectified current shape and making the pulse width of PWM pulses P proportional to the amplified error, the storing and transfer times can be relatively adjusted to make the current shape follow the voltage shape. This causes a reduction in the THD and makes PF unity in the mains current. By making the amplitude of the sinusoidal shaped current proportional to the error between reference voltage V_{set} and the sensed output voltage V_{dc}, good line and load regulation can be obtained. A PI control scheme is used in dc voltage error correction to give good regulation of the output dc voltage.

III. PROPOSED THREE PHASE HIGH PERFORMANCE TELECOM SUPPLY

The control circuit described above is extended to a three phase circuit [9] as in Fig. 5 except for the PI voltage controller, which being at the output, is common to the three phases. The control pulses T1-T4 generated in each phase drive the switches of their respective phase. A 50 kHz triangular wave is common to three phases. This supply configuration is shown in Fig. 5. The supply delivers a dc of $60V_{dc}$, up to 300A to the output load.

IV. PERFORMANCE OF THE CONVERTER

The converter circuit has been optimized for its parameters namely L_1, C_1, C_2, and the integral and proportional controller gains Ki and Kp to give good regulation, low THD, low ripple, unity power factor etc. The main circuit components to be carefully chosen are L_1 and C_2, which have been selected by observing the performance of the converter over a range of values of L_1, C_2 and the converter frequency F_c. The nominal values of L_1 and C_2 have been arrived at assuming a lossless transfer of energy from the mains circuit to the load. Thereafter, the ripple and regulation performance has been simulated in a range of variations of L_1 and C_2 around the nominal values with due checks on the stability of the

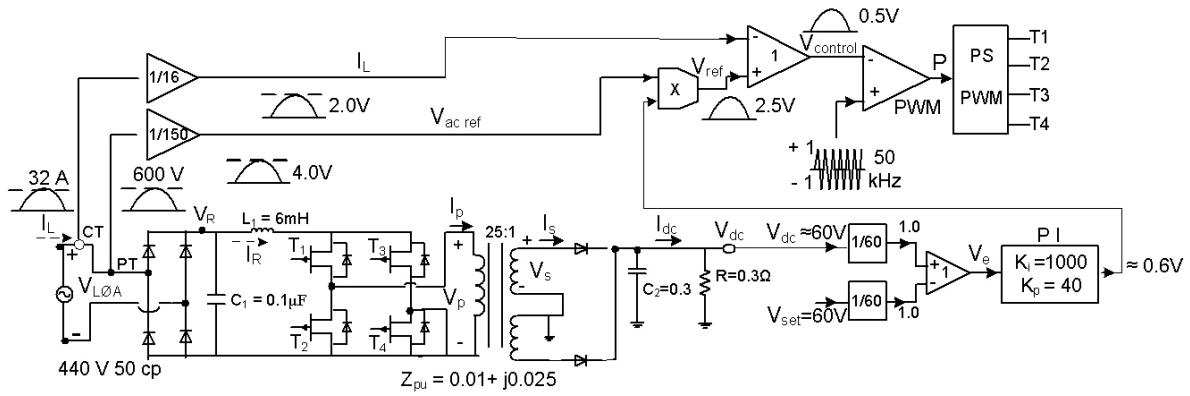


Fig. 3. Control Scheme and Generation of PWM.

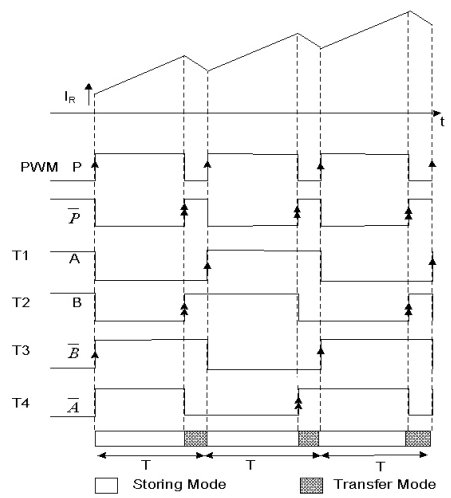


Fig. 4. Current Control via PS-PWM Scheme.

system. It has been observed that L_1 should be within 0.5 to 10 mH for circuit stability. The THD and ripple performance are shown in Fig 6. The best performance is obtained for a value of L_1 that is in the 4 to 6 mH range for frequencies F_c between 5 to 50 kHz.

Similarly for L_1 = 4mH a plot of the THD and ripple voltage vs the converter frequency in Fig. 7 shows that they are low for a frequency F_c between 20 to 50 kHz.

In the same way, the capacitor C_2 is varied between 0.1 and 0.5 F. It has been observed, as shown in Fig 8, that the circuit is stable and the THD is low for a capacitor C_2 that is between 0.2 and 0.7 F. The smaller value of 0.3 F has been chosen in this paper.

Similarly, starting from the nominal values of Ki and Kp these have been fine tuned to give a low rise time and good regulation keeping track of stability. The optimized parameters of the proposed supply at $V_{dc} = 60V$ and $I_{dc} = 200A$ are given in Table I. G's refer to the attenuation of the sampled signals, in the control loop.

TABLE I
OPTIMIZED PARAMETERS VALUES

Circuit Parameters		Transformer Parameters		Control Parameters	
$L_1(mH)$	6	$R(m\Omega)$	3	Ki	1000
$C_1(uF)$	0.1	$L(nH)$	10	Kp	40
$C_2(F)$	0.3	$Rm(k\Omega)$	10	GLi	1/16
$R(\Omega)$	0.3	$Lm(mH)$	100	Grefy	1/150
		$Vsec(V)$ @ Vpri=2kV	40	Gdc	1/60
				Gpid	1
				Gset	1/60
$V_{dc} = 60V,\ I_{dc} = 200A\ @\ V_L = 440Vrms$					

A. Waveforms in the Control Circuit

For the converter circuit values and parameters of the control as per Table I, Fig. 9 shows the simulated waveforms in the converter circuit and control circuit.

The waveform I_R is the rectified mains current in the inductor L_1, duly controlled by PWM. It is characterized by the linear rising and falling profile corresponding to the "storing" and "transfer" modes respectively. The succeeding set of waveforms are made up of the winding voltages and currents in the primary winding V_p, I_p and the secondary winding V_s, I_s of the dc-dc converter. The subscript A denotes that the converter is in phase A of the three phase circuit.

The waveform P is the PWM pulses that have been obtained by a comparison of $V_{control}$ and the 50 kHz triangular wave. Derived from this comparison are the converter switch drive pulses T1 through T4.

1) Waveforms during the Transfer Mode: The waveform T is the transfer mode waveform:

$$T = T1.T4 + T2.T3. \tag{5}$$

When T = '1', the circuit is transferring energy to the load R (I_R is falling) and when it is '0' the energy is being stored in the inductor (I_R is rising).

In the transfer mode, if the primary winding and secondary winding voltage waveforms of the converter in phase A, $V_{P\phi A}$, and V_S are seen, then it is observed that they have a rectangular shape (voltage pulse) since for a short period of the converter switching, V_R at input is constant. The corresponding current

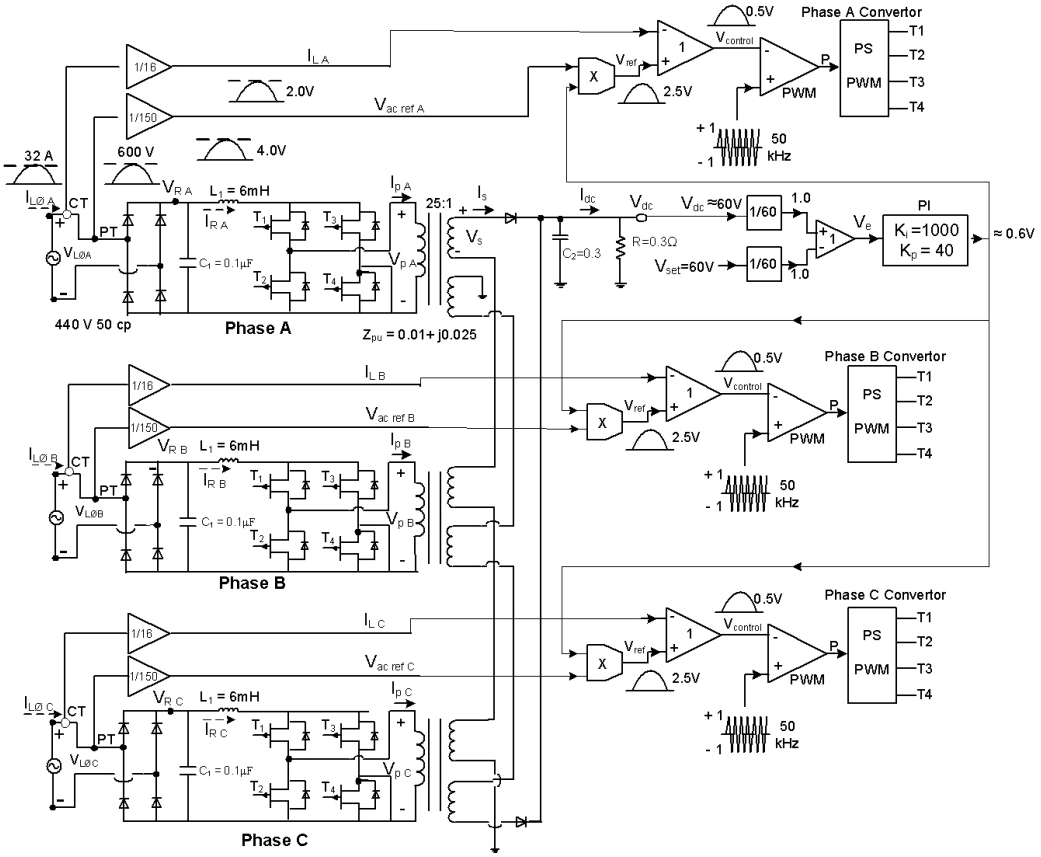


Fig. 5. Three Phase Circuit with PS-PWM Controlled SMR.

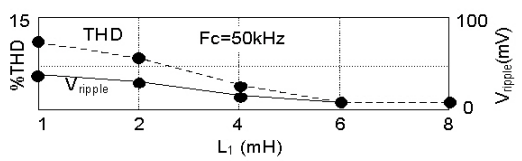


Fig. 6. THD and Ripple Voltage vs L_1.

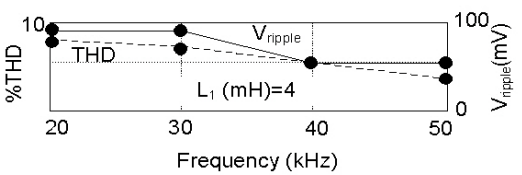


Fig. 7. THD and Ripple Voltage vs frequency F_c.

waveforms of the converter in phase A, $I_{P\phi A}$, I_S are observed (in converter) to have "rising" waveforms, since they are transferring power to the inductive load (transformer) under the action of a rectangular voltage pulse.

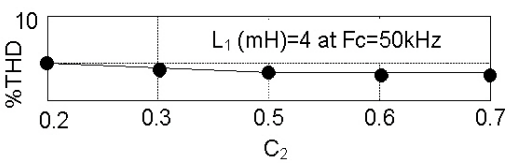


Fig. 8. THD vs Filter Capacitor.

The voltage pulse in the primary winding V_p shows an upward kick at the end of each pulse which is due to the "reverse" current flow from the inductive transformer flowing into the freewheeling diodes or converter switches.

2) Waveforms during the Storing Mode: Since in the PS-PWM scheme the "storing" and "transfer" modes alternate, the time period in which the 'transfer' (waveform) T is low, corresponds to the storing mode. In this period the inductor current I_R increases in value linearly (energy is stored in the inductor L_1). Since in Fig. 9 the storing period is larger than transfer period, the overall value of I_R increases in the waveform from left to right.

Further, since no transfer of the power to the load takes place in the converter during the storing period ('T1 AND T2' OR 'T3 AND T4' are ON shorting the primary winding),

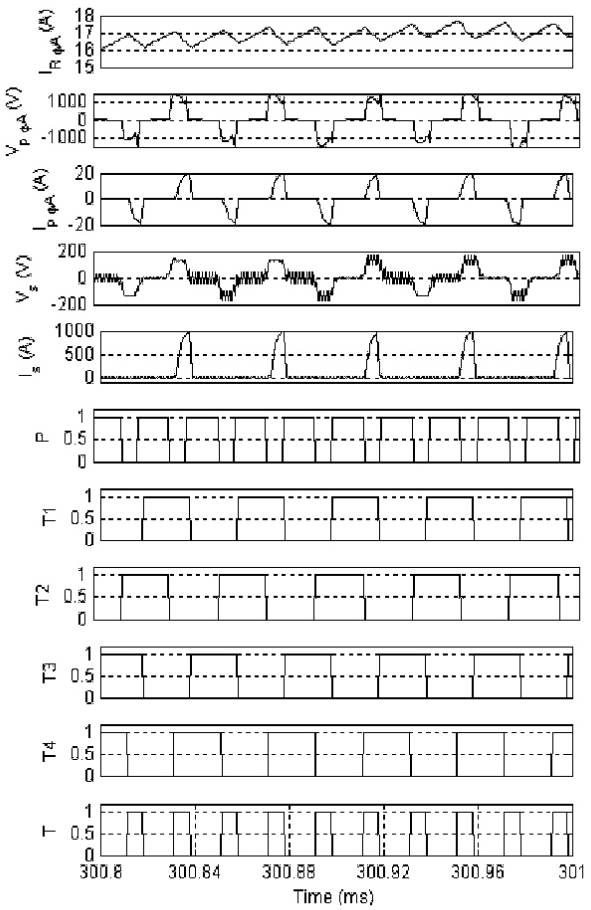


Fig. 9. Converter winding and Control Circuit Waveforms ($V_{dc} = 60V$, $I_{dc} = 200A$, $V_L = 440Vrms$).

the waveforms in the primary and secondary windings have zero value in this period.

B. Behavior of the Phase A, B and C Line Currents

For the optimum values of the converter circuit parameters, given in Table I, the simulated waveforms of line currents in the three phases A, B, and C are shown in Fig 10. It can be seen that the line currents of phases A, B and C ($I_{L\phi A}$, $I_{L\phi B}$ and $I_{L\phi C}$) are equal in magnitude and phase shifted by 120° as balanced line currents. The THD in the line current is less than 4%. Fig. 10 also shows the rectified voltage V_R and current I_R prior to the converter.

C. Load and Line Regulation

Fig. 11 and 12 show numerous simulated waveforms corresponding to the load current $I_{dc} = 100A$ and $300A$. These waveforms show the transient as well as the steady state behavior of the voltages and currents at various nodes in the circuit.

In Fig. 13 and 14 the waveforms are given for the line voltage $V_L = 390V$ and $490V$. The load and line regulation measured from expanded graph is $\approx 50\mu V/A$ and $50\mu V/V$.

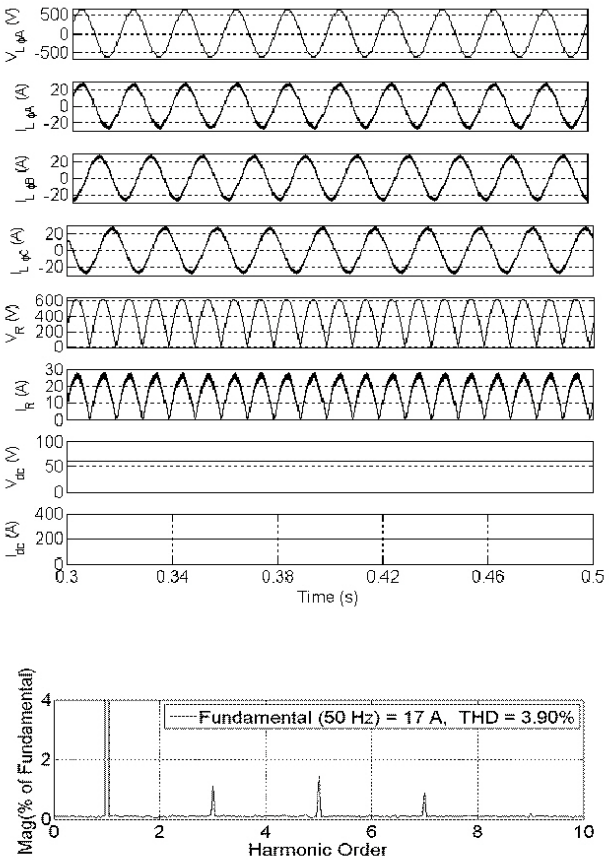


Fig. 10. Waveforms of converter at rated load ($V_{dc} = 60V$, $I_{dc} = 200A$ $V_L = 440V$) voltage and currents in line, mains rectifier, output; and harmonic spectra.

D. Total Harmonic Distortion

Fig. 10 through 14 show the THD and harmonic spectra of the line current. It can be seen that the THD (as a percentage of the rms of the fundamental line current) varies between 7.45% to 3.65% being best in the optimized region of 300 A load and 440 V mains voltage. The percent of harmonic current for the first few harmonics in line A is also shown in these figures.

E. Dynamic Performance

The dynamic performance of the converter has been simulated by switching the load suddenly in the steady state. In Fig 15, the load current is raised from 200 A to 300 A between 0.2 & 0.4 sec. In Fig 16, the load current is switched from 300 A to 50 A between 0.2 & 0.4 sec. In both cases the waveforms of the line current and output currents respond within a half cycle.

V. CONCLUSIONS

A new approach to high performance telecom supply design has been described and validated by MATLAB simulations. The use of a 3-phase supply has permitted the realization of a high power 18 kW, 60 V_{dc} supply with an I_{dc} that is up to 300A. The use of a 3-phase ac mains supply lends

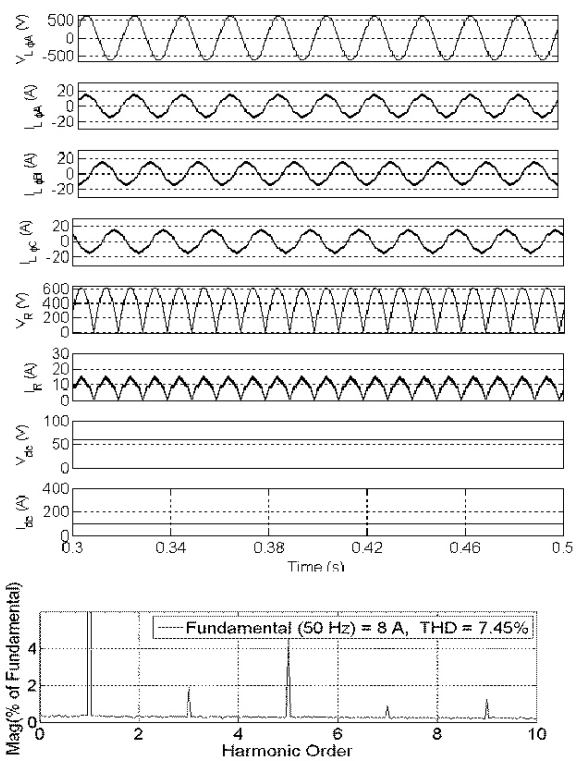


Fig. 11. Load regulation ($V_L = 440V$ $I_{dc} = 100A$) voltage and currents in line, mains rectifier, output; and harmonic spectra.

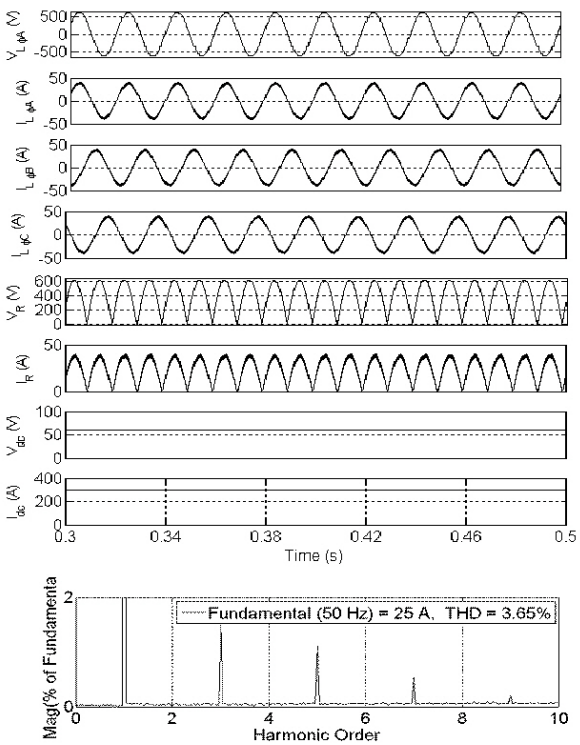


Fig. 12. Load regulation ($V_L = 440V$, $I_{dc} = 300A$) voltage & currents in line, mains rectifier, output; harmonic spectra.

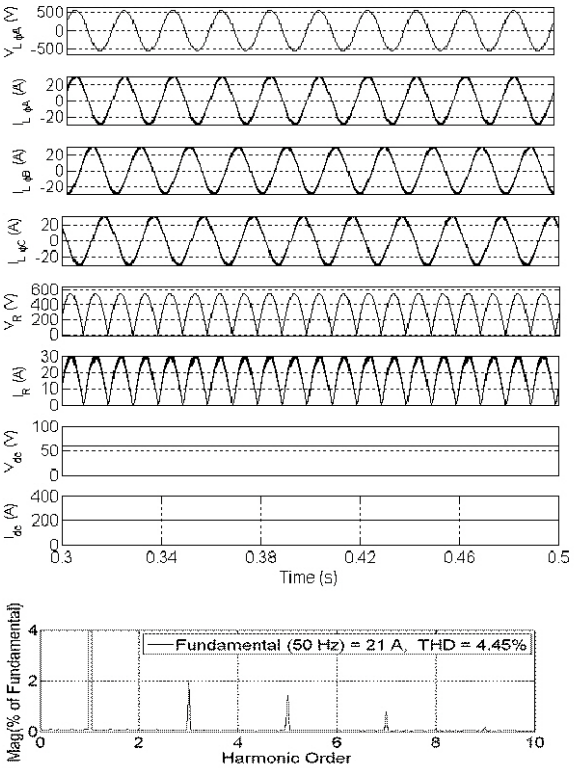


Fig. 13. Line regulation ($V_L = 390V$, $I_{dc} = 200A$) voltage & currents inline, mains rectifier, output; harmonic spectra.

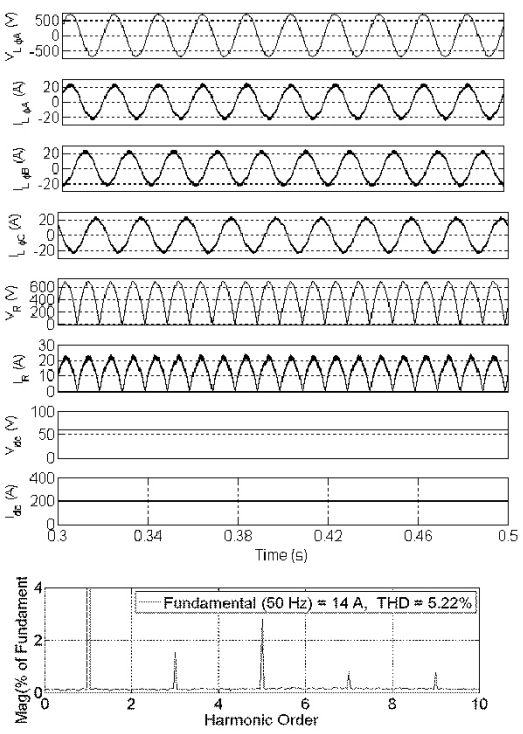


Fig. 14. Line regulation ($V_L = 490V$, $I_{dc} = 200A$) voltage and currents in line, mains rectifier, output; and harmonic spectra.

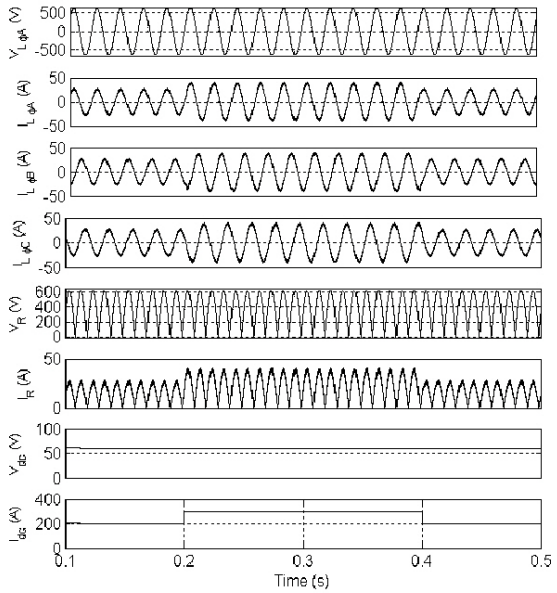


Fig. 15. Dynamic Performance. Load current changed from 200A to 300A.

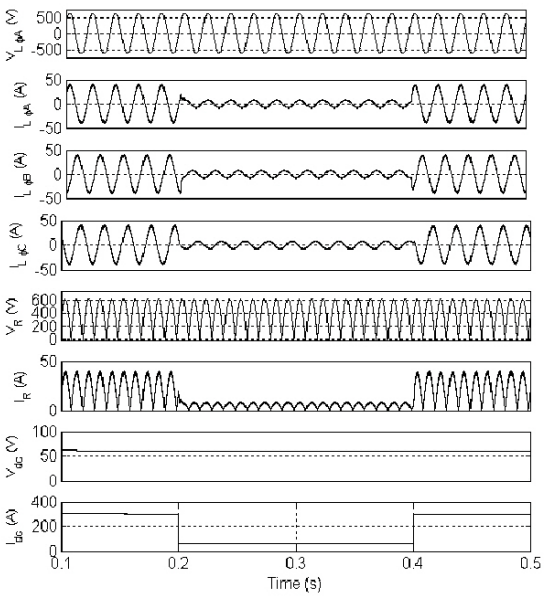


Fig. 16. Dynamic Performance. Load current changed from 300A to 50A.

itself to 6-pulse converters. This is achieved by connecting the converter's secondary windings from individual phases in series.

The technique of switched mode rectification SMR, and phase shifted PWM have been shown to give a sinusoidal line current with a unity power factor and a low THD. The PI voltage controller gives very good line and load regulation.

Extensive simulations have been carried out to give optimum values for the mains rectifier inductor L_1 and the output filter capacitor C_2. Similarly, other parameters have also been optimized carefully and these have been given in Table I. A summary of the performance features for the proposed circuit are given in Table II.

TABLE II
SUMMARY OF KEY FEATURES

	Features	Advantage	Performance
1	Converter Output Series Connected	Balanced 3 phase currents 6 pulse rectifier Low filter capacitor	V_{ripple} pp $\leq$ 50mV
2	PS-PWM Converter Control	Unity pF Low THD	$\approx$ 1.0 $<4\%$
3	PI Voltage Controller	Good load Regulation Good Line Regulation	50μV/A 50 μV/V
4	HF DC-DC Converter	Galvanic Isolation No bulky Mains Transformer	Low Weight
Output: $V_{dc} = 60V$, $I_{dc} = 200A$ Input : Three Phase Mains $440V_{line}$, 50Hz			

The advantages of the newly proposed circuit obtained by a combination of several ideas are summarized below:

Mains current is in phase with the voltage in each phase giving almost unity power factor.

Mains current is almost sinusoidal yielding a low total harmonic distortion.

Three phase circuit currents are balanced.

Galvanic isolation is provided by a compact high frequency converter transformer.

Final output dc is 6 pulse rectified exhibiting low ripple and using a smaller filter capacitor.

Load and line regulation are good.

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