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An Improved Control Approach for DSTATCOM with Distorted and Unbalanced AC Mains

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ABSTRACT

This paper presents a new control approach of DSTATCOM (distribution static compensator) for compensation of reactive power, unbalanced loading and harmonic currents under unbalanced non-sinusoidal ac mains. The control of DSTATCOM is achieved using Adaline based current estimator based on LMS algorithm to maintain source currents real and undistorted. The dc bus voltage of voltage source converter (VSC) working as DSTATCOM is maintained at constant voltage using a proportional-integral (PI) controller. The DSTATCOM system alongwith proposed control scheme is modeled in MATLAB to simulate the behavior of the system. The practical implementation of the DSTATCOM is carried out using dSPACE DS1104 R&D controller having TMS320F240 as a slave DSP. Simulated and implementation results are presented to demonstrate the effectiveness of the DSTATCOM with Adaline based control to meet the severe load perturbations with different types of loads (linear and non-linear) under distorted and unbalanced AC mains.

Keywords: DSTATCOM, Adaline, Harmonic compensation, Load balancing, Unbalanced and Distorted AC Mains

1. Introduction

Compensation of reactive power and unbalance in load current has been a great challenge for power engineers. The adverse effects of low power factor and unbalance loads are increased losses and overloading of one particular phase. These problems are aggravated in harmonic environment, created by power electronics converters [1-3]. These converters do not only corrupt the current but also distort the system voltage. Moreover there is always some amount of voltage unbalance present in the distribution system. Advent of custom power technology has shown the way in form of DSTATCOM (Distribution STATic COMpensator) to meet the load current compensation requirement such as reactive power compensation, load balancing and harmonic elimination. Performance of DSTATCOM system depends on the algorithm used for control of the system so that dynamic compensation of the load can be provided. There are various control algorithms used for detection of reference current for switching of VSC e.g. instantaneous reactive power theory, instantaneous i_d-i_q theory, and method for estimation of current reference by maintaining the voltage of DC bus of DSTATCOM [4-6]. The important requirement for the control algorithm is that it should be simple, easy to implement and work well with non-sinusoidal and unbalanced ac mains, which is a practical situation in present day distribution system for DSTATCOM to work.

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This paper presents the performance of the DSTATCOM system under unbalanced and distorted ac mains conditions for compensation of reactive power, unbalance and harmonic current. The extraction of real balanced fundamental frequency current is carried out using least mean square (LMS) algorithm based ADAptive LInear NEuron (Adaline) [7-8]. This simple and fast Adaline approach is based upon online estimation of weights corresponding to real fundamental frequency current component of load current with minimal time delay. For maintaining the constant voltage at the dc bus of VSC working as DSTATCOM, a PI controller is used. The output of PI controller is added to the weight and this final output is multiplied by the unit voltage templates that have unit amplitude and are in phase with voltage at PCC. Since the voltage at PCC is unbalanced and distorted, for calculation of unit voltage templates, a phased lock loop (PLL) technique is used [9]. These three-phase reference source currents are used to generate switching signals for DSTATCOM using hysteresis based PWM current control method (indirect current control). The indirect current control provides advantage over direct current control as it automatically compensates the delay due to processor and the ripple filter used to suppress the switching frequency noise [10]. The performance of DSTATCOM system is simulated under different load perturbations with distorted and unbalanced ac mains conditions using MATLAB environment along with SIMULINK and PSB Block-set toolboxes. The hardware implementation is carried out to validate the proposed control scheme in real time using dSPACE DS1104 R&D controller.

2. System Configuration

Fig. 1 shows the basic circuit diagram of the DSTATCOM system with lagging power factor linear and nonlinear loads connected to 3-phase, 3-wire distribution system. The three-phase voltage source converter (VSC) working as DSTATCOM is realized using six IGBT (insulated gate bipolar transistor) switches with anti parallel diodes. At dc bus of VSC of DSTATCOM, a dc capacitor is connected. The load currents are tracked by the Adaline based reference current generator and PI controller is used to maintain dc bus voltage of the

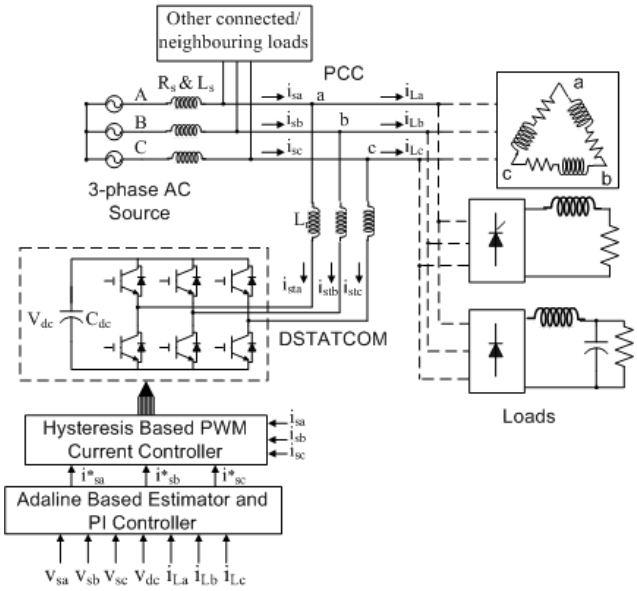


Fig. 1 Basic circuit diagram of the DSTATCOM system

DSTATCOM. This in conjunction with hysteresis PWM current controller provides switching signals for IGBTs of the DSTATCOM. It controls source currents to follow the reference source currents. The system component values are given in Table 1.

Table 1 System Parameters

Supply condition	
Line to line voltage	110V
KVA rating	2kVA
Source impedance	5% with X/R ratio of 10
Frequency	50Hz
DC link Controllers	
PI Gain	K_p=1; K_I=3;
Second order Butterworth filter	f_{cutoff}=150Hz
PLL	
Gains	K_p=100 K_I=3200
Current Controller	
Hysteresis band	0.1A
Switching frequency	12.8 kHz
DSTATCOM	
DC link capacitor	1750μF
Interfacing inductor	2.5mH

3. Control Algorithm

The reference source current used to decide the switching of the DSTATCOM has two parts one is real

fundamental frequency component of the load current, which is being extracted by Adaline and another component, which corresponds to the losses in the DSTATCOM, are estimated using a PI controller. Fig. 2a shows the control scheme of DSTATCOM for the compensation of reactive, unbalanced and harmonic current. The output of the PI controller is added to the weight calculated by the Adaline to maintain the dc bus voltage of the DSTATCOM.

3.1 Extraction of Active Positive Sequence Fundamental Frequency Current from Load Current

The basic theory of the proposed decomposer is based on Least Mean Square (LMS) algorithm [8] and its training through Adaline, which tracks the unit vector templates to maintain minimum error. The basic concept of theory used here can be understood by considering the analysis in single-phase system which is given as under.

For an AC power system the supply voltage may be expressed as:

$$v_s = V_1 \sin \omega t + \sum_{n=2}^{\infty} V_n \sin(n\omega t + \theta_n) \quad (1)$$

The load current, made up of positive sequence active (i_p), reactive (i_q) and negative sequence current (i^-), can be decomposed in parts as:

$$i_L = i_p^+ + i_q^+ + i^- \quad (2)$$

The control algorithm is based on the extraction of current component in phase with the unit voltage template. To estimate fundamental frequency positive sequence active component of load current, the unit voltage template should be in phase with the system voltage and should have unit amplitude further it must be undistorted. Since voltage being distorted, the PLL [9] is used to derive the unit voltage templates. A PLL is a technique which causes one signal to track another one. It keeps an output signal synchronised with a reference input signal in frequency as well as in phase. The outputs of the PLL are sine and cosine signals, these sine and cosine quantities are treated as alpha and beta components and transformed into three phase voltage templates using inverse Clark's transformation.

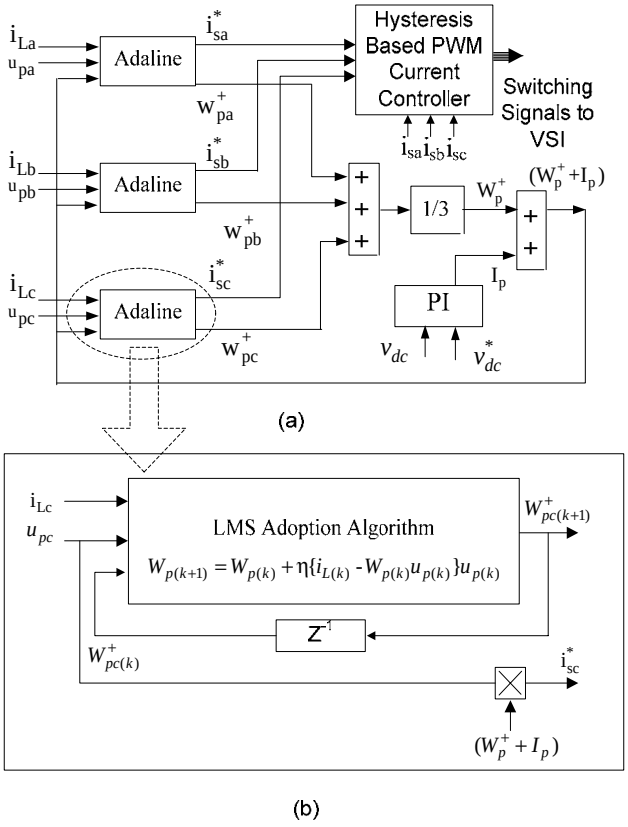


Fig. 2(a)&(b). Basic block diagram of the control for DSTATCOM

The initial estimates of active part of load current for single-phase can be chosen as:

$$i_p = W_p u_p \quad (3)$$

where u_p is unit voltage template and W_p is the weight, which is estimated using Adaline. The weight is variable and changes as per the load current and magnitude of phase voltage. The scheme for estimating weights corresponding to fundamental frequency active component of current (for three-phase system), is based on LMS algorithm. The estimation of weight is given as per the following iterations:

$$W_{p(k+1)} = W_{p(k)} + \eta\{i_{L(k)} - W_{p(k)} u_{p(k)}\} u_{p(k)} \quad (4)$$

This weight is adjusted by the above adaptation rule to keep the output from Adaline $i_{p(k)}$ coinciding with desired output such that the error between the two is minimized. This algorithm is known as Least Mean Square algorithm or Widrow-Hoff delta rule. The value of η (convergence coefficient) decides the rate of convergence and accuracy of estimation. The practical range of convergence coefficient lies in between 0.1 to 1.0. The exact value chosen here is 0.2.

For proper estimation of reference current signals, the weights are averaged to compute the equivalent weight for positive sequence current component in the decomposed form. The averaging of weights helps in removing the unbalance in the current components.

$$W_p^+ = (W_{pa}^+ + W_{pb}^+ + W_{pc}^+)/3 \quad (5)$$

3.2 PI Controller for maintaining constant DC bus voltage of DSTATCOM

To compute the second component of active part reference current, a reference dc bus voltage is compared with sensed dc bus voltage of DSTATCOM. The comparison of sensed dc bus voltage to the reference dc bus voltage of VSC, results in a voltage error, which in the nth sampling instant is expressed as:

$$v_{dcl(n)} = v_{dc(n)}^* - v_{dc(n)} \quad (6)$$

The error signal, $v_{dcl(n)}$, is processed in PI controller and output $I_{p(n)}$ at the n^{th} sampling instant is expressed as:

$$I_{p(n)} = I_{p(n-1)} + K_{pdc}\{v_{dcl(n)} - v_{dcl(n-1)}\} + K_{idc} v_{dcl(n)} \quad (7)$$

where K_{pdc} and K_{idc} are the proportional and integral gains of the PI controller.

The output of PI controller accounts for the losses in DSTATCOM and it is considered as loss component of the current, which is added with the weight estimated by the Adaline corresponding to fundamental frequency positive sequence active reference current component. Therefore, the total real reference current has a component corresponding to the load and a component corresponding to meet the losses of DSTATCOM. It is expressed as:

$$i_{sa}^* = (W_p^+ + I_p)u_{pa};\ i_{sb}^* = (W_p^+ + I_p)u_{pb};\ i_{sc}^* = (W_p^+ + I_p)u_{pc} \quad (8)$$

These 3-phase reference source currents and the sensed source currents are fed to the hysteresis based PWM current controller to force the source currents to follow these reference currents.

Figs. 2a-b show the detailed scheme implemented for the control of DSTATCOM. The structure of Adaline is depicted in Fig. 2b. Weights are averaged not only for averaging at fundamental frequency but these cancel out the sinusoidally oscillating components in weights present due to harmonics in the line. The averaging of weights in different phases is shown in Fig. 2a. Thus Adaline is trained at fundamental frequency of a particular sequence in-phase with voltage. The weights are computed online by LMS algorithm. The update equation of weights based on LMS algorithm is described in (4) for each phase.

Due to the unbalance in the load current the second harmonic ripple is produced in the dc bus voltage. This ripple has to be filtered out before feeding the signal to the PI controller; otherwise this may cause the additional harmonic components in the reference source currents. For this purpose the dc bus voltage is filtered using a low pass filter (LPF). Since the major amount of the reference current (load component) is computed using Adaline based extractor the effect of the delay caused by the LPF used for filtering of dc bus voltage is negligible in practical cases.

4. MATLAB Simulation

For simulation, a MATLAB based block diagram of the model of DSTATCOM system is developed using SIMULINK and Power System Blockset toolboxes. Source block consists of three-phase unbalanced and distorted voltage source, which is modeled using controlled voltage source with source impedance representing a non-stiff source. The linear load is modeled as 0.8 lagging power factor delta connected loads whereas the non linear loads are modeled as three-phase thyristor converter and diode rectifier feeding power to resistive

load with filters at dc side. DSTATCOM is modeled using IGBT switch assembled in form of voltage source converter with the dc capacitor connected at the dc bus. Simulation of the DSTATCOM system is carried out using ode45(stiff/NDF) solver with a maximum step size of 1×10^{-6} sec and relative tolerance 1×10^{-3} under continuous mode.

5. Hardware Implementation

The hardware implementation of control scheme of DSTATCOM system is realized through dSPACE DSP processor. The load currents of a and b-phases (i_{La} and i_{Lb}) are sensed using a Hall effect current sensors (LEM CT-100S). Since the implementation is carried out for 3-phase 3-wire system, third phase current is calculated by considering the sum of three currents zero. Similarly another set of current sensors are used to sense source currents of a and b-phases (i_{sa} and i_{sb}). Three voltage sensors (LEM CV3-1500) are used to sense phase-a, phase-b and dc link voltages. These signals sensed from the sensors are fed to this scaling circuits consisting of fast operational amplifiers (OP-07). The outputs of scaling circuit are given to ADCs of the dSPACE card. The software implementation of control algorithm is realized in MATLAB blocks in DSP dSPACE to generate the switching signals for IGBTs of DSTATCOM using Adaline based reference current extraction technique and hysteresis PWM current controller. These switching signals are fed to SKHI 22B drivers, which finally provide the gate voltage at the gate terminal of the IGBT module (SKM 100GB128DN). For implementation, the control algorithm is run at fixed step size of 78.125μs. The interfacing inductor value is chosen to be 3mH and the value of dc bus capacitor is kept 1650μF.

6. Results and Discussion

Simulation of the DSTATCOM system is performed for different source and load conditions. The source conditions, which are considered here, are unbalanced ac mains, distorted ac mains and unbalanced and distorted ac mains. Operation of DSTATCOM to meet the requirement of reactive, harmonic current compensation with load balancing is demonstrated for both linear and nonlinear type of loads. Following observations are made on the basis of obtained simulation results under different system conditions.

6.1 Unbalanced and distorted ac mains with linear load

Performance of the DSTATCOM system with distorted and unbalanced ac mains feeding power to linear load is shown in Fig. 3. Three-phase quantities such as voltages at PCC, source currents, load currents, DSTATCOM currents and dc bus voltage of DSTATCOM are shown in this figure as v_{pcc}, i_s, i_l, i_{st} and v_{dc} respectively. The unbalanced and distorted source voltage causes load currents to be distorted and unbalanced even if the load impedance offered is equal in all three phases. The unbalance is due to the less voltage of phase a (55.1V), it is 12.3% less as compared to the healthy phases (63.5V). The load perturbation is shown at t=0.12sec by increasing load. From source currents, it is evident that the DSTATCOM is able to compensate the load perturbations within one cycle of sine wave. At t=0.18sec the load from one leg of delta connected load is taken out and it can be seen that the DSTATCOM is able to keep source currents balanced. At t=0.24sec single phasing of the load is shown by taking out the second leg of delta connected load. The DSTATCOM is able to balance source currents and reduce its %THD (1.02%) as compared to that of the load current (2.44%) as depicted in Table 2. The corresponding harmonic spectrum of the PCC voltage, load current and source current for phase a is shown in Figs. 4 (a)-(c).

6.2 Unbalanced and distorted ac mains with non-linear load

With distorted and unbalanced ac mains conditions two types of nonlinear loads; thyristor based ac-dc converter and diode rectifier, are considered. Two different kind of non-linear loads are investigated as the diode rectifier does not consume reactive currents where as the reactive power demand of the thyristor converter depends on the thyristor firing angle. Fig. 5 shows the results of dynamic performance of the DSTATCOM system with unbalanced and distorted ac mains voltage supplying to a thyristor

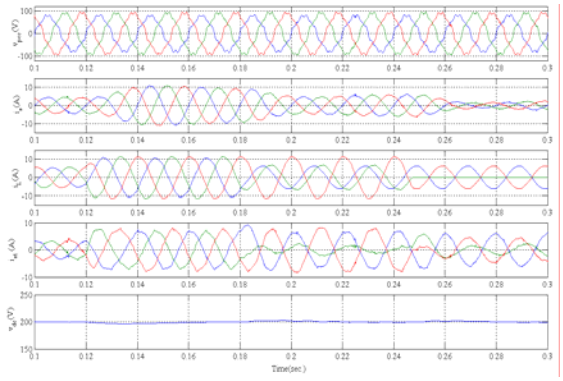
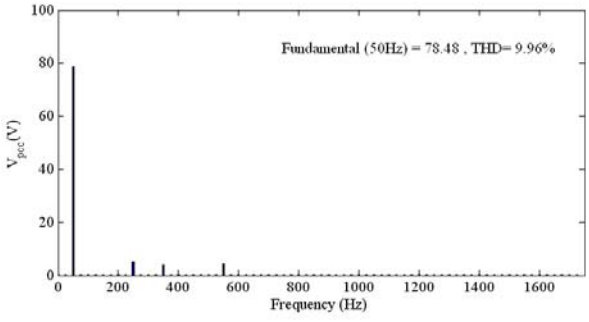
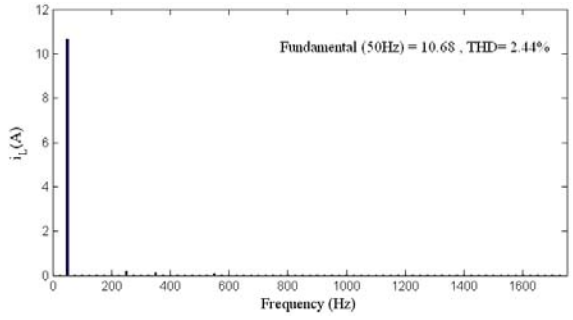


Fig. 3 Dynamic performance of the DSTATCOM system with unbalanced and distorted source voltage and linear load



(a)



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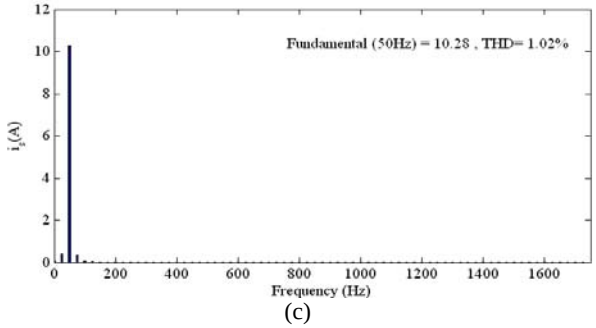


(c)

Fig. 4 Harmonic spectra of (a) source voltage, (b) load current and (c) source current for unbalanced and distorted mains feeding to linear load at full load condition

converter (at 15^o firing angle) feeding to a resistive load.

Upto t=0.12 sec the thyristor converter is working at light load condition and at t=0.12 load is increased. Harmonic and reactive current compensation is shown during this time period, for various conditions of the loads, to keep the source current real and sinusoidal at fundamental frequency. At t=0.18 sec the load in phase a is taken out and single phasing is demonstrated. It is clearly seen from the waveforms of the source currents that DSTATCOM is able to keep the source currents sinusoidal and balanced. The harmonic spectra of the phase a voltage, load and source currents are shown in Figs. 6 (a)-(c) and tabulated values of the %THD and peak fundamental values are given in Table 2. Similarly for diode rectifier, the performance of DSTATCOM is simulated for unbalance and distorted ac mains condition. Fig. 7 shows the various waveforms depicting the performance of the DSTATCOM compensating for diode rectifier. Figs. 8 (a)-(c) show the harmonic spectrum of the voltage, load current and source current and the tabulated values of all the phases are given in Table 2. DSTATCOM is fulfilling the requirement of IEEE-519 standard as the %THD values of the source currents are almost in between 3% to 4%, which is less than the limit prescribed by this standard.

6.3 Experimental results

Test results of the developed prototype of DSTATCOM having rating of 1.8kVA is presented in this section as a to verify the effectiveness of the control to cater power

Table 2 %THD and Fundamental RMS values of voltage at pcc, load current, source current under balanced full load condition

Condition (at full load)		% THD			Fundamental RMS (V or A)		
		Ph. a	Ph. b	Ph. c	Ph. a	Ph. b	Ph. c
Unbalanced and distorted voltage with linear load	v_{pcc}	10.0	8.5	8.4	55.3	63.3	63.2
	i_L	2.4	2.2	2.2	7.4	8.0	8.0
	i_S	1.0	1.5	1.6	7.2	7.2	7.2
Unbalanced and distorted voltage with thyristor converter	v_{pcc}	10.0	8.8	8.7	55.1	63.2	63.1
	i_L	30.2	28.7	29.4	7.4	7.7	7.6
	i_S	3.4	4.8	3.6	8.4	8.3	8.3
Unbalanced and distorted voltage with diode rectifier	v_{pcc}	9.9	8.6	8.6	55.2	63.2	63.2
	i_L	66.3	67.6	69.9	5.8	6.2	6.6
	i_S	1.6	2.3	2.1	6.4	6.4	6.4

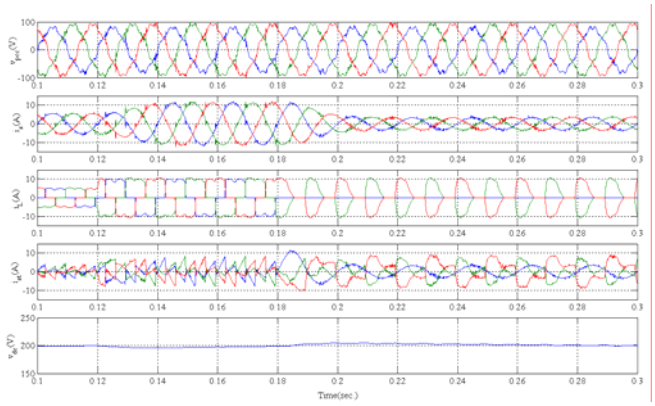


Fig. 5 Dynamic performance of the DSTATCOM system with unbalanced and distorted source voltage and thyristor converter as non-linear load

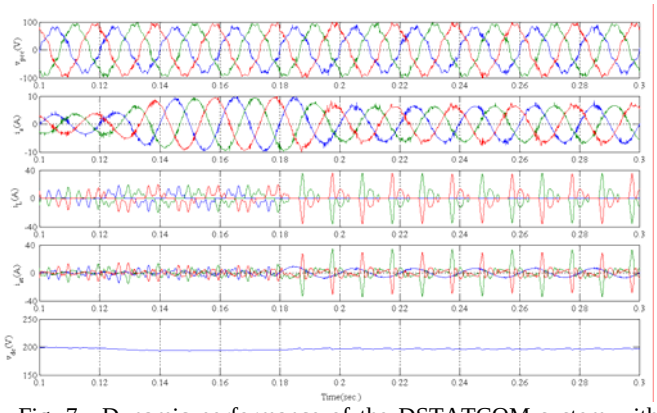
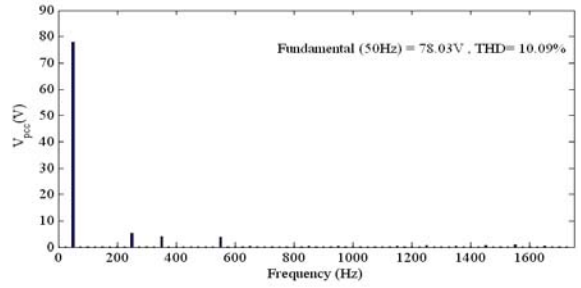
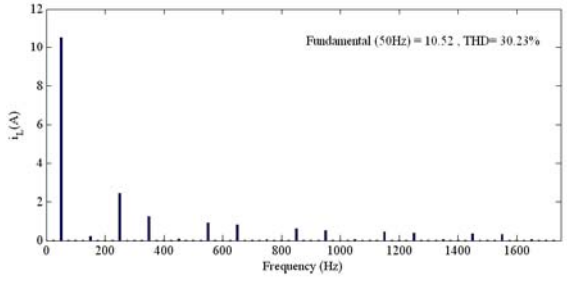


Fig. 7 Dynamic performance of the DSTATCOM system with unbalanced and distorted source voltage and diode rectifier as non-linear load



(a)



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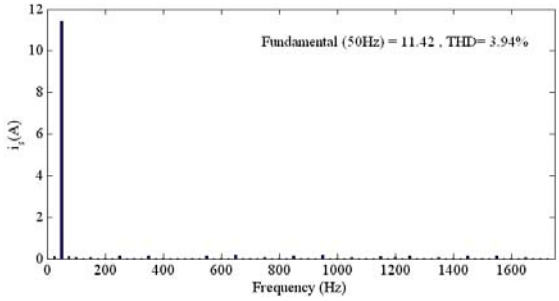
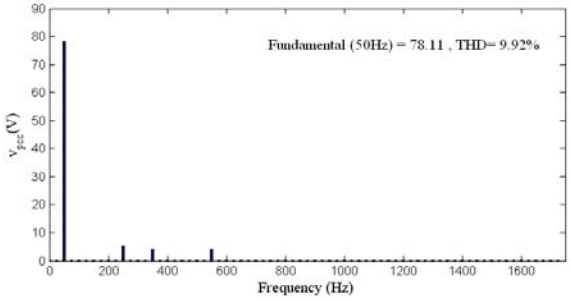
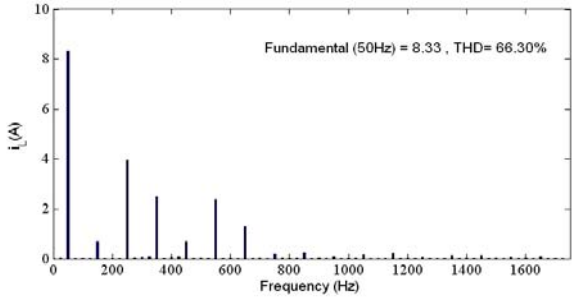


(c)

Fig. 6 Harmonic spectra of (a) source voltage, (b) load current and (c) source current for unbalanced and distorted mains feeding to thyristor



(a)



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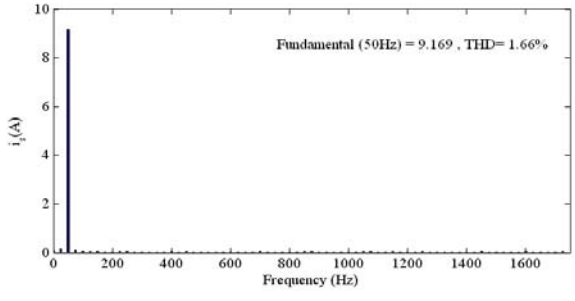


(c)

Fig. 8 Harmonic spectra of (a) source voltage, (b) load current and (c) source current for unbalanced and distorted mains feeding to diode rectifier at full load condition

quality problems. The high source impedance with nonlinear load results in distortion in voltage at PCC. For distortion in voltage is as high as 7.1%. The harmonic spectra of load and source currents are presented in Fig. 14

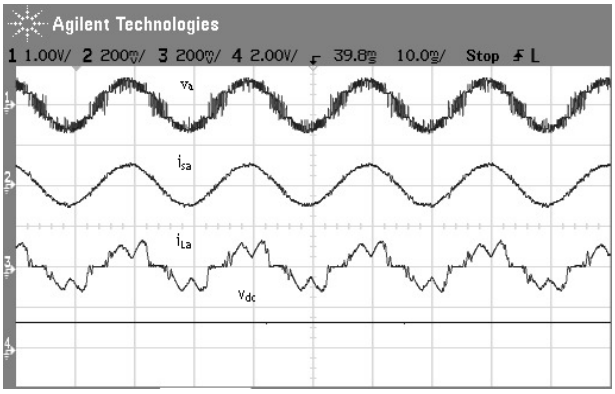


Fig. 9 Steady state wave forms of compensation by DSTATCOM under distorted ac mains. (Scales: 150V/div for channel 1 and 20A/div for channel 2, & 3 and300V/div for channel 4)

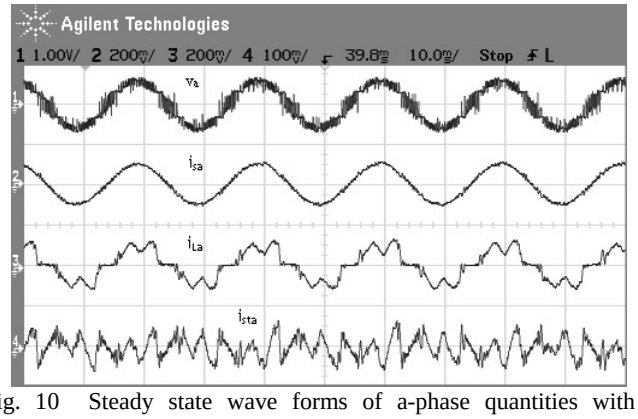


Fig. 10 Steady state wave forms of a-phase quantities with non-linear load under distorted ac mains. (Scales: 150V/div for channel 1 and 20A/div for channel 2, 3 & 10A/div for channel 4)

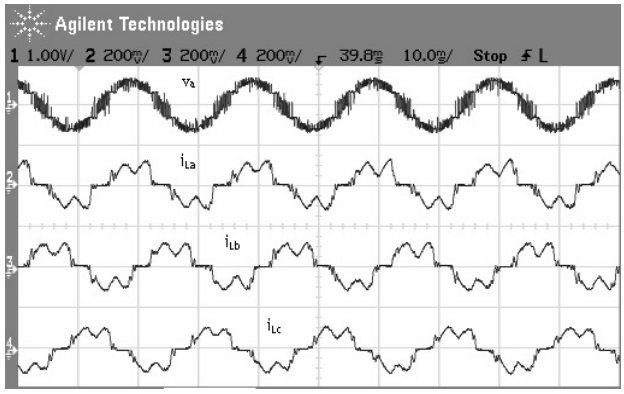


Fig. 11 Wave form of three-phase load currents with non-linear load under distorted ac mains. (Scales: 150V/div for channel 1 and 20A/div for channel 2, 3 & 4)

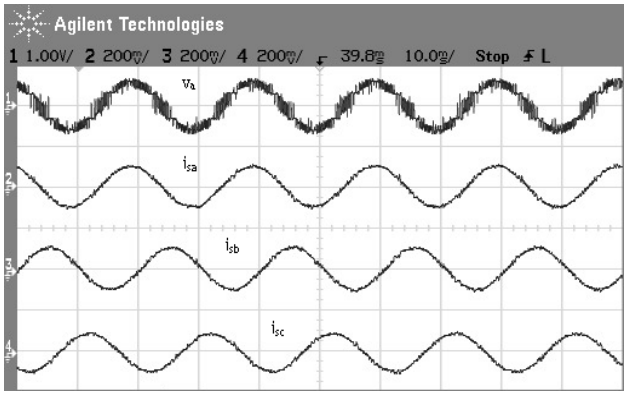


Fig. 12 Wave form of three-phase source currents with non-linear load under distorted ac mains. (Scales: 150V/div for channel 1 and 20A/div for channel 2, 3 & 4)

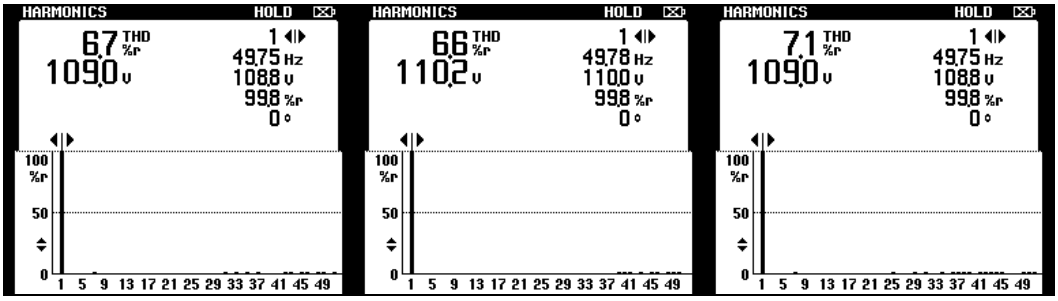
increasing the voltage distortion an extra nonlinear load is connected at PCC. The steady state waveforms demonstrating compensating characteristics of the DSTATCOM under distorted ac mains are shown in Fig. 9. This figure shows the distorted a-phase voltage with source current, load current and dc link voltage. Fig. 10 shows a-phase quantities i.e. voltage, source current, load current and compensating current. Three-phase load currents along with a-phase voltage are shown in Fig. 11. The waveforms of three-phase source currents are given in Fig. 12.

The harmonics spectra of three-phase line to line voltages are shown in Figs. 13(a)-(c). The total harmonic and Fig. 15. The THD in load current is nearly 30%. The harmonic spectra of source currents illustrate that the distortion is well below the limits and Adaline based control scheme is able to provide load compensation even if the ac mains voltage is distorted.

7. Conclusions

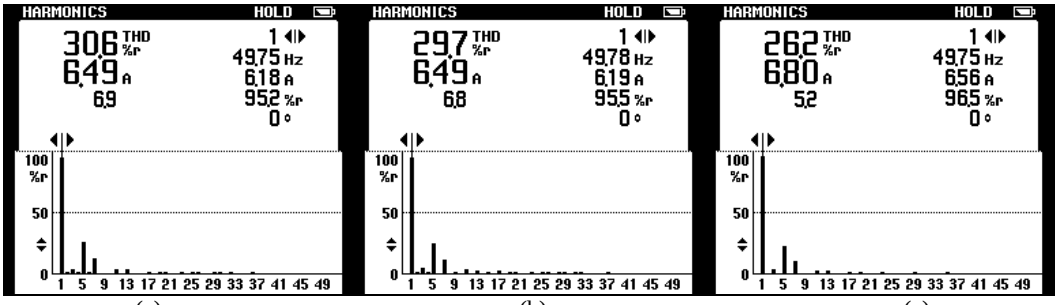
The effectiveness of the DSTATCOM with the proposed control technique has been demonstrated to meet severe load change under unbalance conditions even if the source voltage is unbalanced and distorted. The DSTATCOM with proposed control scheme is able to

balance the source currents and keeps it at fundamental frequency by providing harmonic compensation for extreme unbalanced condition of the load. The control



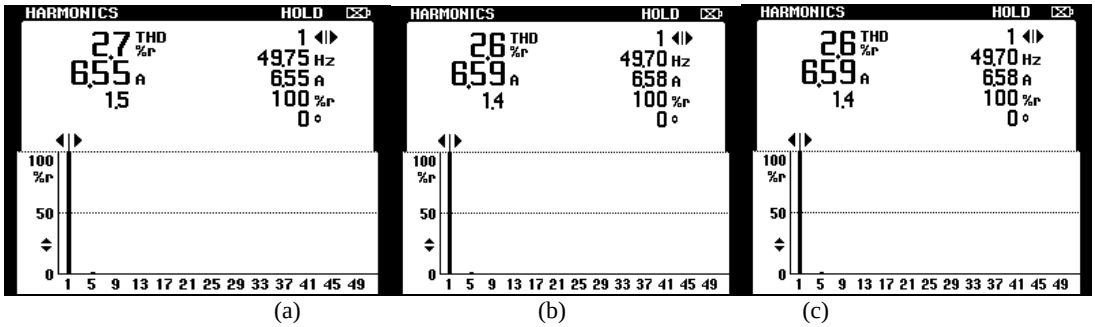
(a) (b) (c)

Fig. 13 Harmonic spectra of L-L (a) ph-a to ph-b voltage, (b) ph-b to ph-c voltage and (c) ph-c to ph-a voltage



(a) (b) (c)

Fig. 14 Harmonic spectra of (a) a-phase load current, (b) b-phase load current and (c) c-phase load current



(a) (b) (c)

Fig. 15 Harmonic spectra of (a) a-phase source current, (b) b-phase source current and (c) c-phase source current

algorithm has envisaged nearly zero phase shift to extract the reference currents with simplicity.

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