

Analysis of a Harmonics Neutralized 48-Pulse STATCOM with GTO Based Voltage Source Converters

Bhim Singh* and Radheshyam Saha[†]

Abstract – Multi-pulse topology of converters using elementary six-pulse GTO - VSC (gate turn off based voltage source converter) operated under fundamental frequency switching (FFS) control is widely adopted in high power rating static synchronous compensators (STATCOM). Practically, a 48-pulse (6x8 pulse) configuration is used with the phase angle control algorithm employing proportional and integral (PI) control methodology. These kinds of controllers, for example the ± 80 MVAR compensator at Inuyama switching station, KEPCO, Japan, employs two stages of magnetics viz. intermediate transformers (as many as VSCs) and a main coupling transformer to minimize harmonics distortion in the line and to achieve a desired operational efficiency. The magnetic circuit needs altogether nine transformers of which eight are phase shifting transformers (PST) used in the intermediate stage, each rating equal to or more than one eighth of the compensator rating, and the other one is the main coupling transformer having a power rating equal to that of the compensator. In this paper, a two-level 48-pulse ± 100 MVAR STATCOM is proposed where eight, six-pulse GTO-VSC are employed and magnetics is simplified to single-stage using four transformers of which three are PSTs and the other is a normal transformer. Thus, it reduces the magnetics to half of the value needed in the commercially available compensator. By adopting the simple PI-controllers, the model is simulated in a MATLAB environment by SimPowerSystems toolbox for voltage regulation in the transmission system. The simulation results show that the THD levels in line voltage and current are well below the limiting values specified in the IEEE Std 519-1992 for harmonic control in electrical power systems. The controller performance is observed reasonably well during capacitive and inductive modes of operation.

Keywords: Fundamental frequency switching, Gate-Turn off thyristor, Phase shifting transformer, Total harmonic distortion, Voltage source converter

1. Introduction

Multi-pulse multi-level GTO-VSC based STATCOM with GTO triggering once per cycle of fundamental system frequency is a matured technology [1-21] and is currently being commercially used by utilities. For example, the ± 80 MVAR Static VAR compensator (SVG) at Inuyama 154kV Switching station, Kansai Electric Power Co. (KEPCO), Japan [3], the ± 100 MVAR STATCOM at TVA Sullivan 161/500kV Substation, Tennessee, USA [4],[8] and the ± 160 MVA STATCOM under the AEP UPFC project [10] have been designed and developed with 48-pulse, 2-level GTO-VSC topology employing eight elementary 6-pulse VSCs and two stages of magnetics. A set of intermediate transformers (as many as VSCs) as part of a first stage are connected to the converter terminals, and a main coupling transformer as part of a second stage

of magnetics is interfacing the intermediate transformers with the line at the point of common coupling (PCC). A 48-stepped and close to sinusoidal AC output voltage waveform is achieved at the point of coupling by adding electro-magnetically the square wave voltage output waveforms of 8x6-pulse VSC bridges, which contains harmonics in the order of $6NP \pm 1$, where P is the number of six-pulse VSCs (eight) and $N=1, 2, 3, 4, \dots$ etc. Thus, in the existing 8x6 pulse 2-level compensator [3], there are nine transformers that include eight series connected intermediate transformers, each with a minimum capacity (MVA) equal to one-eighth of the compensator rating, and one main coupling transformer unit rated with the same capacity as that of the compensator. This cluster of transformers provides the equivalent leakage reactance to control active and reactive power flow in the system.

In this paper, a 48-pulse 2-level, ± 100 MVAR STATCOM device employing eight elementary 6-pulse GTO-VSCs operated at FFS is modeled and simulated with a design of single stage of magnetics to obtain a harmonic neutralized and close to sinusoidal AC output voltage waveform by means of SimPowerSystems toolbox in MATLAB environment.

[†] Corresponding Author: Central Electricity Authority, Sewa Bhawan, R. K. Puram, New Delhi-110 066, India (email:rshahacno@yahoo.com)

* Department of Electrical Engineering, Indian Institute of Technology, New Delhi-110 016, India (email:bhimsinghr@gmail.com)

Received: 31 October, 2007 ; Accepted: 3 June, 2008

In the proposed STATCOM, there is no requirement of intermediate transformers and only four transformers including three numbers of PSTs providing phase shifts of -15° , $+15^\circ$, and $+30^\circ$ are designed to electro-magnetically add the converters output at PCC. The interference of the triplen harmonic components in the line is also minimized by designing the primary windings of the 30° PST. In the control algorithm, simple PI controllers in voltage and current control loops are adopted in d-q rotating frame reference for control of the converter phase angle (α) voltage in respect of the line voltage across the leakage reactance. This STATCOM is tested for voltage regulation in an electrical network supplying power to a reactive load and its design and MATLAB-simulation results are illustrated in this paper.

2. Working Principle of STATCOM

The main objective of STATCOM is to control reactive current by generation and absorption of controllable reactive power with various solid-state switching techniques. While the basic architecture, working principle, and operating characteristics of STATCOM have been widely explained in the literature [3], [6], [7], [9], the salient aspect of GTO-VSC based STATCOM to be operated in FFS mode is briefly illustrated in Figs. 1a-1b. The essential components in a GTO-VSC based STATCOM are GTO-VSC bridge(s), DC capacitor (C) working as an energy storage device, interfacing magnetics forming the electrical coupling between the VSC bridge circuits and AC system, and a phase angle (α) controller for generating gating signals.

A controllable three-phase 48-pulse AC output voltage waveform is obtained by means of phase angle control at PCC. AC output voltage of VSC bridge circuits, V_c

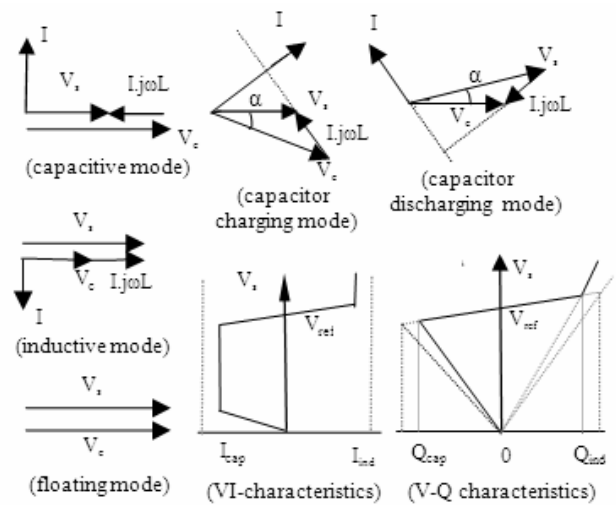


Fig. 1b. STATCOM operating characteristics.

(cumulative AC output voltage of multiple converters) is governed by DC capacitor voltage (V_{dc}), which can be controlled by varying phase difference between V_c (converter output fundamental voltage) and V_s (system voltage at PCC). An almost sinusoidal current in quadrature (I) with the line voltage is injected into the electrical system by the STATCOM emulating an inductive or a capacitive reactance. The magnitude and phase difference between V_c and V_s across the transformer leakage inductance (L) controls the reactive and active power flow. Fig. 1b shows the basic operating characteristics of a GTO-VSC based STATCOM. When $V_c > V_s$, the STATCOM is considered to be operating in a capacitive mode and when $V_c < V_s$, it is operating in an inductive mode and for $V_c = V_s$, no reactive power exchange takes place and STATCOM is operated in floating mode.

3. Model of STATCOM

Fig. 2 shows the circuit layout of the proposed 48-pulse STATCOM configuration. The 48-pulse model is achieved by 8×6 -pulse GTO-VSCs that are connected in parallel on the DC side with an energy storing DC capacitor ($4000\mu\text{F}$). Eight 6-pulse VSCs to be operated at FFS are divided into four pairs and they are operated at phase displacement angles of $(-11.25^\circ, 161.25^\circ)$, $(3.75^\circ, 176.25^\circ)$, $(18.75^\circ, 191.25^\circ)$, and $(33.75^\circ, 206.25^\circ)$. The outputs from each pole of the four VSC pairs are fed at opposite ends of the open wye secondaries of the four transformers whose primaries are connected in series on the line side to electro-magnetically add the outputs from the four pairs of VSCs. Thus, a composite multi-pulse voltage waveform of 48-steps with a displacement angle of 7.5° is achieved at the PCC through the proposed four transformers employed as a single stage of magnetics.

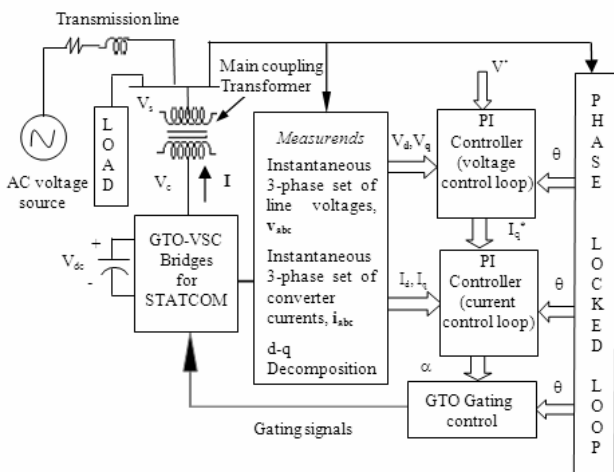


Fig. 1a. GTO-VSC based STATCOM architecture and working principle.

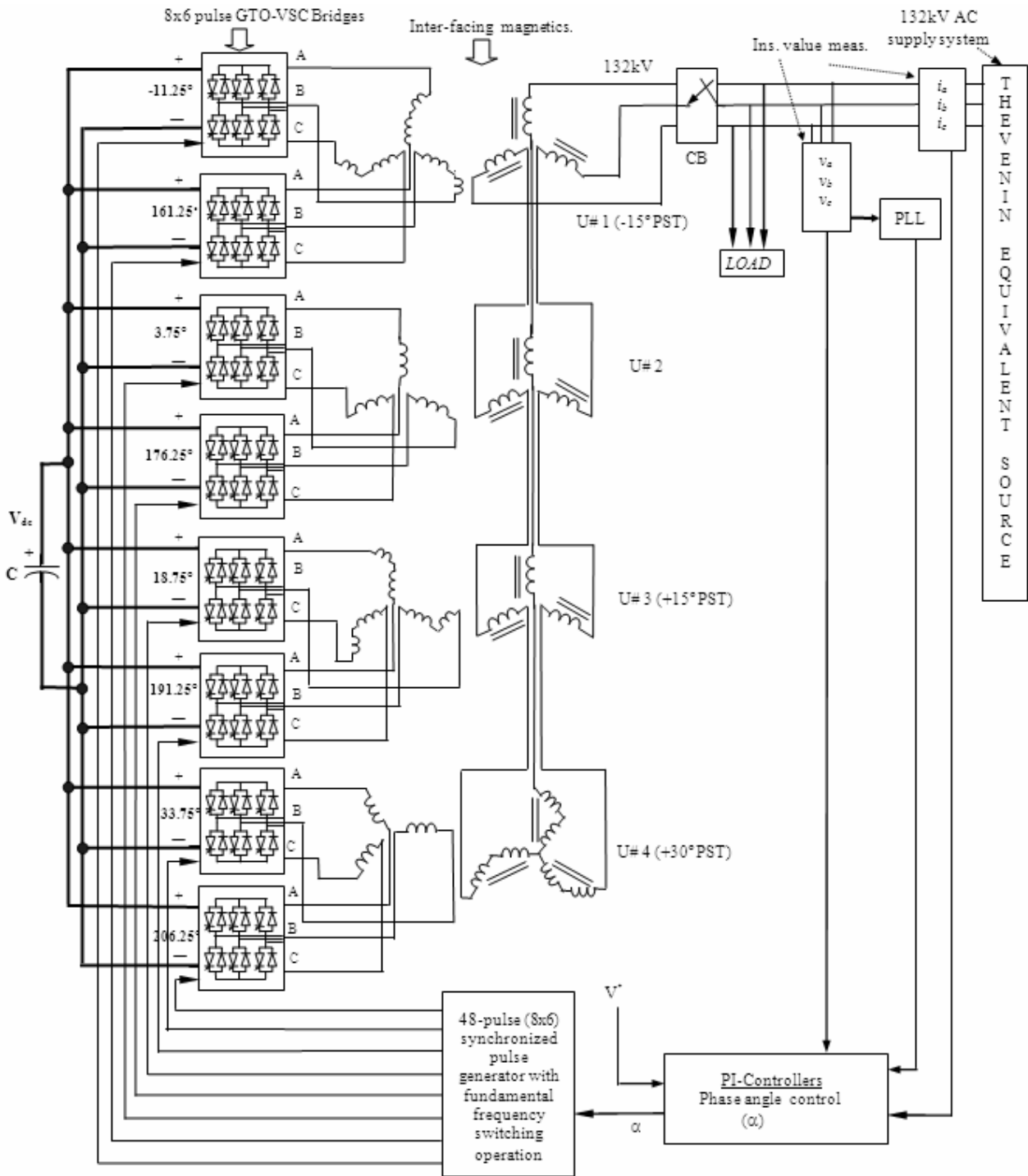


Fig. 2. System configuration of 8X6 pulse + 100MVAR GTO-VSC based STATCOM.

Out of the four transformer units (U#1,2,3,4), the first (U#1), third (U#3), and fourth (U#4) units are PSTs providing phase shift of -15° , $+15^\circ$, and $+30^\circ$, respectively. The -15° and $+15^\circ$ PSTs are designed with open-wye primary and zig-zag connected open-wye secondary connections whereas the $+30^\circ$ PST is configured with zig-zag/inter-connected star as primary and open-wye as secondary. The transformer unit (U#2) is a normal 3-phase

2-winding step-up transformer having open-wye secondary and open-wye primary terminals. The phase-displaced output from each pole of the first VSC pair (-11.25° , 161.25°) is fed into the opposite ends of open-wye secondaries of the U#1, the output from the second VSC pair (3.75° , 176.25°) fed into the opposite ends of open-wye secondaries of the U#2, the output from the third VSC pair (18.75° , 191.25°) fed into the opposite ends of open-

wye secondaries of the U#3, and the output from the fourth VSC pair (33.75°, 206.25°) fed into the opposite ends of open-wye secondaries of the U#4. The transformers' primaries (U#1, 2, 3 and 4) are connected in series to electro-magnetically add the outputs from the four pairs of VSC bridge circuits enabling the achievement of a harmonic neutralized output having forty-eight steps of voltage output waveform with an evenly displaced step size of 7.5° at PCC.

The AC mains system is represented by Thevenin voltage source with a short-circuit level of 3000 MVA and X/R ratio equal to 10. An inductive load of 70MW, 0.85pf is considered to regulate voltage across it at various set point reference voltages.

The PI-control algorithm to be used in the control scheme is illustrated in Fig. 3, which is comprised of two PI-control loops viz. outer voltage control loop and inner current control loop. The outer voltage loop determines the reference reactive current (i_q^*) for the compensator and the inner control loop determines α to generate the gating pulses. The AC line voltages (v_{abc}) and converter current (i_{abc}) signals (instantaneous values) are sensed in time domain and transformed into the d-q reference frames i.e. $v_d - v_q$ and $i_d - i_q$ respectively.

The Phase Locked Loop (PLL) is employed to calculate phase and frequency information of the fundamental positive sequence component of the system voltage, which synchronizes AC output voltage of the VSCs. The magnitude of the line voltage (V_{dq}) calculated from the value of v_d and v_q is compared to the reference voltage, V^* and the error signal is controlled to obtain the reference reactive current (i_q^*). The value of i_q^* is then compared with

i_q^* in the inner current loop and the error signal is controlled to generate desired phase angle (α). The proportional (K_p 's) and integral gains (K_i 's) of the two control loops are tuned to control load voltage in the system.

3.1 Interfacing Magnetics

The interfacing magnetic circuits comprising of the four transformers are shown in Fig. 2 and their detail design parameters are provided in the Appendix. The 15°-lag PST (U#1) and 15°-lead PST (U#3) are configured by employing a 3-winding linear transformer per phase with two sets of windings on its secondary side and single-winding on the primary side. Three such transformers for each PST are employed to obtain six open-wye terminals in their primaries and six open-wye terminals in their secondaries. The winding turns of secondaries and primaries of the U#1 and U#3 are determined to obtain the desired phase shifts; the secondaries are fed from the poles of the VSC pairs (-11.25°, 161.25°) and (18.75°, 191.25°), respectively. Figs. 4a and 4c illustrate the winding configurations of the U#1 and U#3, respectively.

The second transformer (U#2) requiring no phase shift is configured with a two-winding linear transformer per phase and three such transformers are employed to obtain six open-wye configurations in primary and secondary terminals; the secondaries are fed from the poles of the VSC pair (3.75°, 176.25°). Fig. 4b illustrates the winding configuration of the transformer.

A 3-phase 30° lead PST (U#4) as shown in Fig. 4d is modeled by employing a 3-winding linear transformer per phase and three such transformers are employed for the 3-phase model. The double-winding side constitutes the primary side to be utilized for zigzag or interconnected star connection and the single-winding side constitutes the secondary side providing 6-terminal open-wye connection. The winding turns of the primaries and secondaries are derived to obtain the desired phase shift of 30° lead. The primary winding is constituted with two halves of the same number of turns having opposite hands of windings that are connected in zig-zag fashion so that the voltage across two of them joined in series is the difference of the voltages in each half with a phase shift of +30°. The secondaries are fed from the poles of the VSC pair (33.75°, 206.25°).

The interconnection of the four sets of transformers with primary sides connected in series on the line side and secondaries connected to the four VSC pairs forms the single-stage model of the interfacing magnetics which enables the electro-magnetic addition of the outputs from the four pairs of VSC bridge circuits to obtain a 48-stepped voltage output waveform at the PCC with an evenly displaced step size of 7.5°. The resulting AC voltage waveform has only 48N±1 harmonics i.e. 47th, 49th, etc.

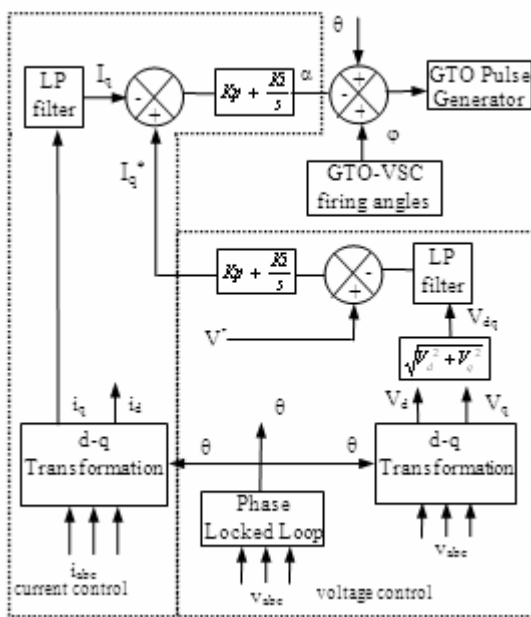
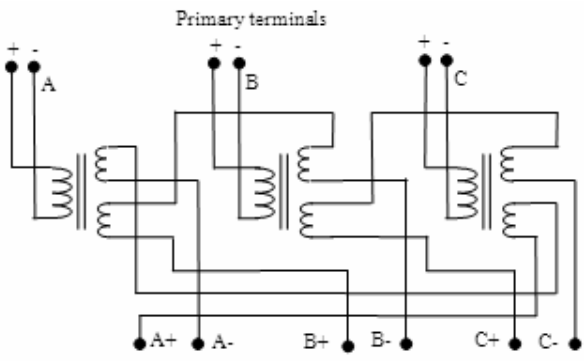
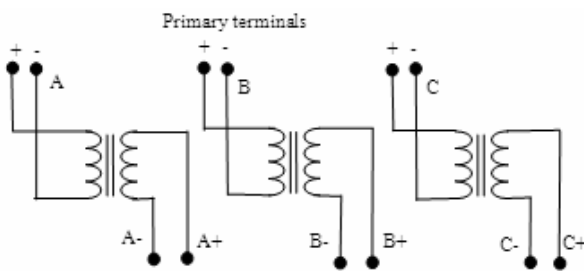


Fig. 3. Control Scheme.



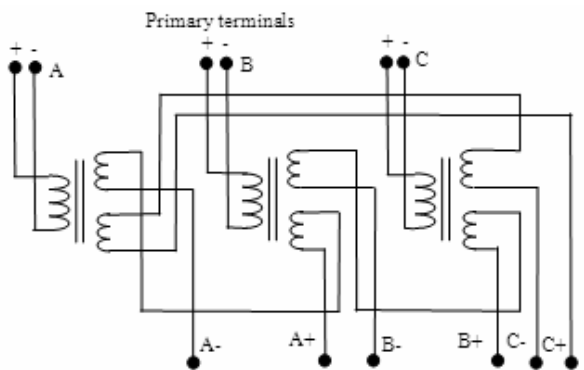
Input from the VSC pair triggered at angles of 18.75° and 191.25°

Fig. 4a. 15° lag PST (U#1).



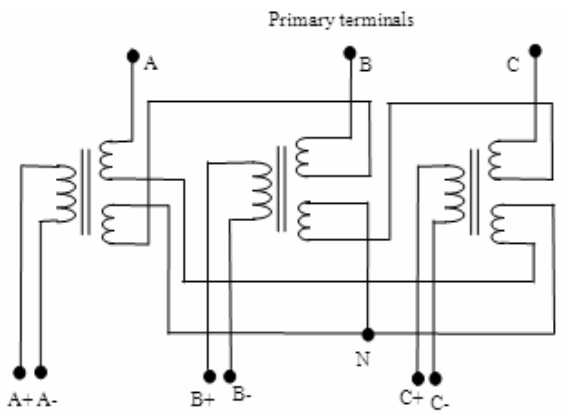
Input from the VSC pair operated at angles 3.75° and 176.25°

Fig. 4b. Transformer (U#2).



Input from the VSC pair triggered at angles -11.25° and 161.25°

Fig. 4c. 15° lead PST (U#3).



Input from the VSC pair triggered at angles 33.75° and 206.25°

Fig. 4d. 30° lead PST (U#4).

4. MATLAB Simulation Results and Discussion

The AC multi-stepped output voltage waveform across the terminals (open) of the proposed 48-pulse STATCOM model as obtained from the MATLAB simulation results is shown in Fig. 5. The operating performance characteristics of the compensator corresponding to the capacitive and inductive modes of its operation are illustrated under steady state and dynamic operating conditions.

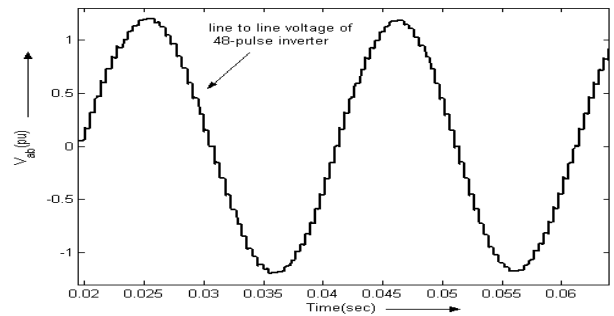


Fig. 5. 48-pulse STATCOM AC output voltage waveform at PCC.

4.1 Steady State Operation

In the simulation model, voltage regulation at an inductive load of 70MW 0.85pf lag in the network has been studied. With the reference line voltage V^* set to 1.0pu, 1.03pu, and 0.97pu at the instant of 0s, 0.22s, and 0.42s respectively, the capacitive reactive current limit is set to $I_q^* = 1.2pu$ and the inductive reactive current limit at $I_q^* = -1.2pu$ in the voltage control loop. With the DC capacitor (C) pre-charged and total simulation time set at 0.62sec, the performance of the compensator under the floating, capacitive and inductive modes of operation has been observed. Phase voltages (v_a, v_b, v_c) and supply current characteristics (i_a, i_b, i_c) corresponding to the specific time intervals are shown in Fig. 6. The operating characteristics of other system variables e.g. $V_{ab-pcc}, (V_a, I_a)$,

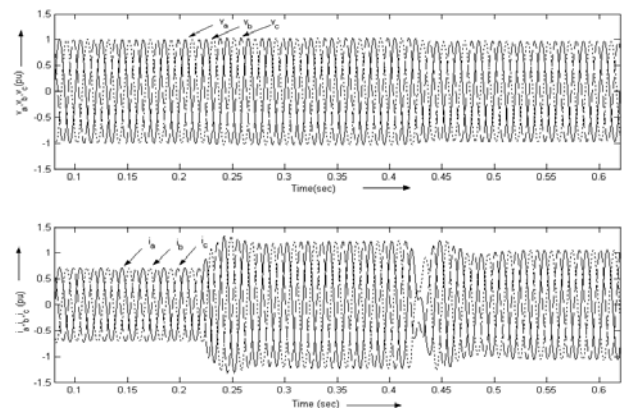


Fig. 6. Three-phase instantaneous supply voltage $v_a, v_b,$ and v_c and load current $i_a, i_b,$ and i_c .

(V^* , V_{dq}), V_{dc} and (α , I_q^* , I_q) in respect of time (sec) are shown in Fig. 7.

It is observed that during the interval 0-0.22s (reference voltage set at $V^*=1.0pu$) both the active power and reactive power requirements of the load are met from the AC supply. As well, the line voltage (decomposition value of the load voltage, V_{dq}) is seen closely following the reference voltage.

During the interval (0.22s-0.42s) when V^* is set to 1.03pu, it is seen from the (v_a , i_a) and (V^* , V_{dq}) characteristics (Fig. 7) that the supply current i_a leads v_a and the external voltage loop controller is producing the desired reference reactive current (I_q^*) for the current loop while maintaining a constant line voltage at its reference value ($V^*=1.03pu$) emulating the compensator as a capacitive reactance. Similarly, during the interval (0.42s-0.62s) when V^* is set to 0.97pu, it is seen from the (v_a , i_a) and (V^* , V_{dq}) characteristics (Fig. 6) that the supply current i_a lags v_a with the controller regulating the reference reactive current (I_q^*) within limits to maintain the constant line voltage at its reference value ($V^*=0.97pu$) emulating the compensator as an inductive reactance.

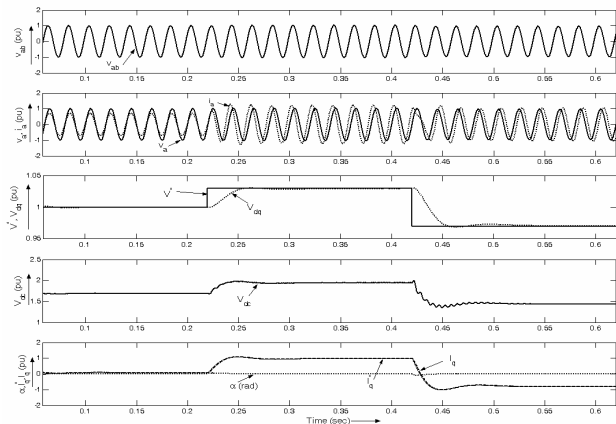


Fig. 7. Operating characteristics of STATCOM at 70MW 0.85pf (lag) load condition in voltage control mode.

4.2 Dynamic Characteristics

It is seen from Fig. 7 that while reference voltage V^* is dynamically changed in the simulation from 1.0 pu to 1.03 pu and from 1.03pu to 0.97pu at the instant of 0.22s and 0.42s respectively, the compensator responds within a couple of cycles during which time both the conditions and controller provides necessary damping to rapidly settle to steady state conditions enabling smooth operation of the system. No major overshoots or undershoots in voltage and current transients have been observed from the operating characteristics.

The results of FFT analysis on voltage and current spectra are illustrated in Figs. 8a-8d. Table-1 provides the

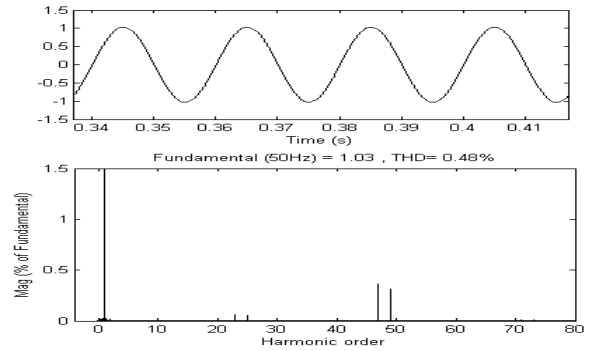


Fig. 8a. Harmonic spectrum of phase-a voltage (v_a) in capacitive mode.

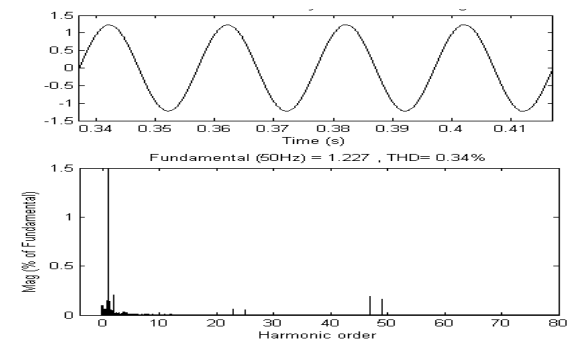


Fig. 8b. Harmonic spectrum of phase-a current (i_a) in capacitive mode.

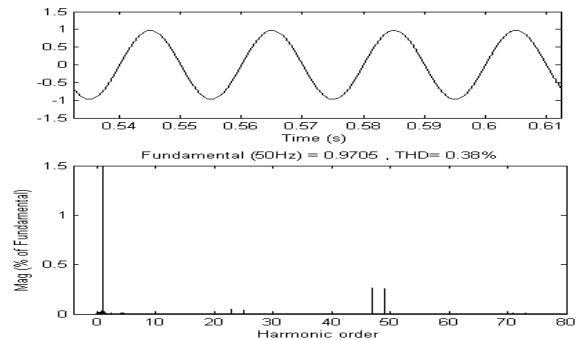


Fig. 8c. Harmonic spectrum of phase-a voltage (v_a) in inductive mode.

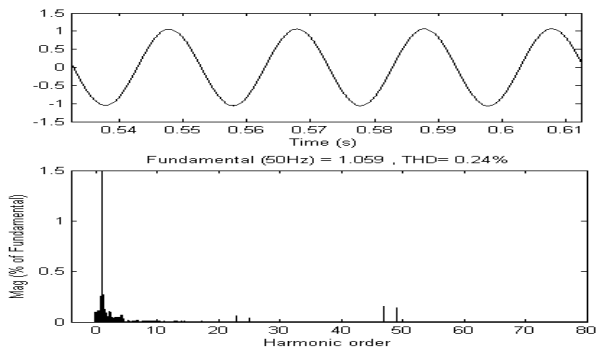


Fig. 8d. Harmonic spectrum of phase-a current (i_a) in inductive mode.

Table 1. Summary of Voltage and Current Harmonics.

Proposed STATCOM	Voltage Harmonics			Current Harmonics		
	Magnitude (%)		Overall %THD	Magnitude (%)		Overall %THD
Capacitive mode	3 rd	nil	0.48%	3 rd	0.01%	0.34%
	5 th , 7 th	nil		5 th , 7 th	0.01%	
	9 th	nil		9 th	0.01%	
	11 th , 13 th	nil		11 th , 13 th	nil	
	15 th	nil		15 th	0.01%	
	17 th , 19 th	nil		17 th , 19 th	nil	
	21 st	nil		21 st	nil	
	23 rd	0.06%		23 rd	0.07%	
	25 th	0.05%		25 th	0.05%	
		
47 th	0.36%	47 th	0.19%			
49 th	0.31%	49 th	0.16%			
Inductive mode	3 rd	nil	0.38%	3 rd	0.04%	0.24%
	5 th , 7 th	nil		5 th	0.01%	
	9 th	nil		7 th	0.02%	
	11 th , 13 th	nil		9 th	0.01%	
	15 th	nil		11 th , 13 th	0.01%	
	17 th , 19 th	nil		15 th	0.01%	
	21 st	nil		17 th , 19 th	nil	
	23 rd	0.05%		21 st	nil	
	25 th	0.04%		23 rd , 25 th	0.04%	
		
47 th	0.27%	47 th	0.16%			
49 th	0.26%	49 th	0.14%			

summary results of various voltage and current harmonic components and overall THD (Total Harmonic Distortion) values during capacitive and inductive modes of operation of the compensator. It is observed that voltage THD lies in the range of 0.38% - 0.48% and current THD is 0.24% - 0.34%.

4.3 Zero Sequence Voltage and Current Mitigation

Zero sequence voltage/current harmonic components are minimized by designing the primary windings of the +30° PST (U#4). Employing a zig-zag/inter-connected star connection in the primary with its two winding halves configured with opposite hands of windings and connected in series, the direction of current flow in the two halves/windings has been reversed which enables minimization of the 3rd, 9th, 15th, etc. voltage/current harmonics (triplens) in the line. The fundamental voltage phasor diagrams of the primary and secondary circuits are shown in Fig. 9.

Fig. 10 illustrates the instantaneous phase current (i_{pu}) waveforms of the transformer secondaries (U#1-4), which are closely sinusoidal in nature during the various operating modes of the compensator. Magnitudes of the zero sequence harmonic components (i.e. 3rd, 9th, 15th, etc.) of the phase current in the 30° PST (U#4) as obtained from the MATLAB-simulation results are summarized in Table-2 and it is observed that triplen current components have been attenuated.

From Fig. 7, showing instantaneous phase voltage and current (v_a , i_a) characteristics, and Figs. 8a-8d, showing

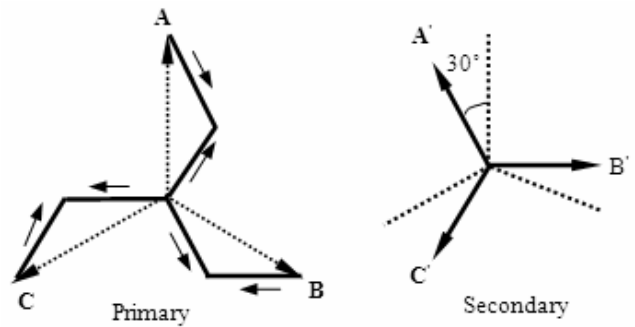


Fig. 9. Fundamental voltage phasor diagrams of primary and secondary voltages of the 30° PST (U#4).

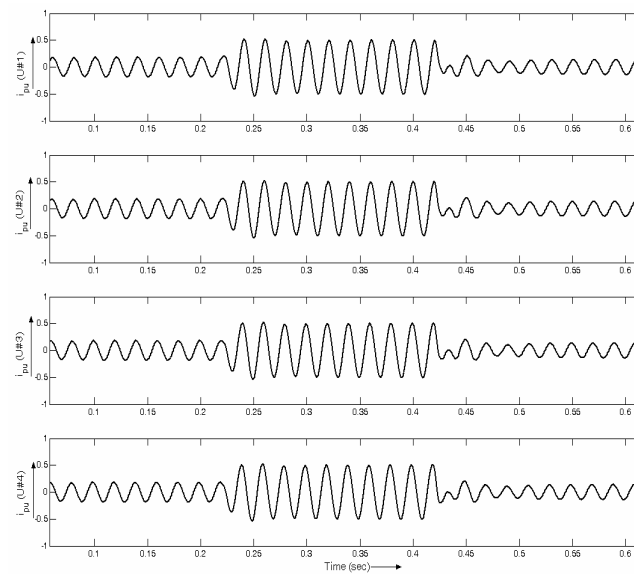


Fig. 10. Current waveforms of transformer secondaries (U#1, 2, 3, 4).

Table 2. Secondary current harmonics (triplens) components of the 30° PST (U#4).

Proposed STATCOM	Current harmonics (triplen) and magnitude (%)	Overall %THD in secondary current
Capacitive mode	3 rd - 0.05% 9 th - 0.01% 15 th - 0.01%	0.4%
Inductive mode	3 rd - 0.10% 9 th - 0.06% 15 th - 0.03%	0.97%

harmonic spectra corresponding to capacitive and inductive modes of operation of the STATCOM, it has been observed that the impact of zero sequence harmonics currents in the line are insignificant.

5. Conclusion

A 48-pulse two-level GTO-VSC based ± 100 MVAR, 50Hz, 132kV STATCOM has been modeled in MATLAB environment by using 8x6-pulse VSCs operated on FFS principle and phase angle control algorithm employing PI-controllers. With the use of eight numbers of six-pulse converters, interfacing magnetics have been conceptualized and designed in single stage in the compensator circuit instead of the conventional two stages topology adopted in the high power rating 48-pulse STATCOM [3],[4],[8],[10]. This compensator has been configured for voltage regulation in the high voltage 132kV system. Under single stage configuration of magnetics, the overall capacity requirement (MVA) of the magnetics has been optimized to half of that needed in the commercially available compensator and thus, becomes cost effective. The number of transformers in the magnetic circuit has been reduced from nine [3] to four. With the standard PI-control algorithm adopted in the inner current control and outer voltage control loops, the compensator has enabled smooth control of load voltage in the system under various operating conditions and it has provided the damping to rapidly settle to steady state condition. The presence of lower and higher order harmonics in both line voltage and current has been found to be appreciably low, and THD levels are well within the IEEE Std. 519-1992 operating limits [22]. The impact of zero sequence harmonics has been neutralized by adopting the zig-zag configuration of the 30° PST in the magnetic circuit.

Appendix

Parameters of the GTO-VSC based 48-pulse, 2-level, ± 100 MVAR STATCOM model:

STATCOM Parameters:

Converter Type-VSC; Thyristors - GTO; No.of pulses - 48; Nominal AC voltage - 5.1kV; Nominal DC voltage - 8.3kV; GTO fixed resistance-0.01 Ω ; GTO triggering control at fundamental frequency (50Hz); DC Capacitor - 4000 μ F.

Interfacing magnetics (Base-100MVA):

Transformer (U # 1):

3-phase 3-winding zigzag connected (-) 15° PST
Rating: 25MVA, 50Hz, 33 kV/10.2kV, 8% (X)
Vector group: Y/zigzag-Y

Transformer (U # 2):

3-phase 2-winding step-up transformer (no phase shift)

Rating: 25MVA, 50Hz, 33kV/10.2kV, 8% (X)
Vector group: Y/Y

Transformer (U # 3):

3-phase 3-winding zigzag connected (+) 15° PST
Rating: 25MVA, 50Hz, 33 kV/10.2kV, 8% (X)
Vector group: Y/zigzag-Y

Transformer (U # 4):

3-phase 3-winding (+) 30° PST
Rating: 25MVA, 50Hz, 10.2/(33/ $\sqrt{3}$) kV, 8% (X)
Vector group: zigzag or interconnected-star/Y

PI-controller gains:

Inner current controller: $K_p=38, K_i=350$

Outer voltage controller: $K_p=70, K_i=1500$

The equivalent voltage source:

Nominal voltage: 132kV (rms); System frequency-50Hz
Short circuit level: 3000MVA; X/R ratio-10

Transmission line:

$R=0.1622\Omega, L=1.0214e-3H$

Discrete sampling time for simulation = 5e-6s

MATLAB Version – 6.5 (Release 13)

References

- [1] E. J. Stacey, "Simplified quasi-harmonic neutralized high power inverters," U. S. Patent 4 870 557, Sept. 26, 1989.
- [2] C. D. Schauder, "Advanced Static VAR Compensator Control System," U. S. Patent 5 329 221, Jul. 12, 1994.
- [3] S. Mori, K. Matsuno, T. Hasegawa, S. Ohuichi, M. Takeda, M. Seto, S. Murakami, and F. Ishiguro, "Development of a large static VAR generator using self-commutated inverters for improving power system," *IEEE Trans. on Power Systems*, vol. 8, no. 1, pp. 371-377, Feb. 1993.
- [4] C. Schauder, M. Gernhardt, E. Stacey, T. Lemak, L. Gyugyi, T. W. Cease, and A. Edris, "Development of a ± 100 MVAr static condenser for voltage control of transmission systems," *IEEE Trans. on Power Delivery*, vol. 10, no. 3, pp. 1486–1496, July 1995.
- [5] C. K. Lee, Joseph S. K. Leung, S. Y. Ron Hui, and Henry Shu-Hung Chung, "Circuit-level comparison of STATCOM technologies," *IEEE Trans. on Power Electronics*, vol. 18, no. 4, pp. 1084–1092, July 2003.

- [6] G. C. Cho, G. H. Jung, N. S. Choi, and G. H. Cho, "Analysis and controller design of static VAR compensator using three-level GTO inverter," *IEEE Trans. on Power Electronics*, vol. 11, no. 1, pp. 57 – 65, Jan. 1996.
- [7] J. E. Hills and W. T. Norris, "Exact analysis of a multipulse shunt converter compensator or STATCOM Part-I and II: Performance," *IEE Proc. Generation, Transmission and Distribution*, vol. 144, no. 2, 1997, pp. 213-218 and 219-224.
- [8] C. Schauder, M. Gernhardt, E. Stacey, T. Lemak, L. Gyugyi, T. W. Cease, and A. Edris, "Operation of $\pm 100\text{MVAR}$ TVA STATCON," *IEEE Trans. on Power Delivery*, vol. 12, no. 4, pp. 1805-1811, Oct. 1997.
- [9] K. K. Sen, "Statcom - static synchronous compensator: theory, modeling, and applications," *IEEE PES WM 1999*, vol. 2, pp. 1177 –1183.
- [10] C. Schauder, L. Gyugyi, E. Stacey, M. Lund., L. Kovalsky, A. Keri, A. Mehraban, and A. Edris, "AEP UPFC project: installation, commissioning and operation of the $\pm 160\text{MVA}$ STATCOM (phase-I)," *IEEE Trans. on Power Delivery*, vol. 13 no. 4, pp. 1530 –1535, Oct. 1998.
- [11] Y. H. Liu, J. Arrillaga, and N. R. Watson, "Multi-level voltage reinjection – a new concept in high voltage source conversion," *IEEE Proc., Generation Transmission and Distribution*, vol. 151, no. 3, 2004, pp. 290-298.
- [12] Y. H. Liu, J. Arrillaga, and N. R. Watson, "STATCOM performance of a multi-level voltage reinjection converter," *IEEE/PES Transmission and Distribution Conference & Exhibition: Asia and Pacific*, 2005.
- [13] M. S. El-Moursi, and A. M. Sharaf, "Novel Controllers for the 48-Pulse VSC STATCOM and SSSC for voltage regulation and reactive power compensation," *IEEE Trans. on Power Systems*, vol. 20, no. 4, pp. 1985-1987, Nov. 2005.
- [14] Y. H. Liu, R. H. Zhang, J. Arrillaga, and N. R. Watson, "An overview of self-commutating converters and their application in transmission and distribution," *IEEE/PES Trans. and Distrib. Conf. & Exhibition: Asia and Pacific*, 2005.
- [15] K. R. Padiyar and Nagesh Prabhu, "Design and performance evaluation of sub-synchronous damping controller with STATCOM," *IEEE Trans. on Power Delivery*, vol. 24, no. 3, pp. 1395 –1405, July 2006.
- [16] A. Jain, K. Joshi, A. Behal, and N. Mohan, "Voltage regulation with STATCOMs: modeling, control and results," *IEEE Trans. on Power Delivery*, vol. 21, no. 2, pp. 726-735, Apr. 2006.
- [17] B. K. Panigrahi, M. K. Mallick, and S. S. Dash, "A novel fuzzy logic controller for STATCOM to improve power system stability," *Int. Journal of Automation and Control*, vol. 1, no. 1, pp. 4-15, 2007.
- [18] B.-S. Chen and Y.-Y. Hsu, "An analytical approach to harmonic analysis and controller design of a STATCOM," *IEEE Trans. on Power Delivery*, vol. 22, no. 1, pp. 423-432, Jan. 2007.
- [19] W. Pan, J. Zhang, H. Chen, Y. Chang, and C. Wang, "Novel configuration of 60 pulse voltage source converter," *IEEE PES GM*, 2007.
- [20] N. Voraphonpiput, I. Ngamroo, and S. Chatratana, "Control system design for a STATCOM using complex transfer function," *WSEAS Int. Conf. Proce. on Instrumentation, Measurement, Circuits & System*, 2007, pp. 186-192.
- [21] Z. Xi, and S. Bhattacharya, "STATCOM operation strategy under power system faults," *IEEE PES GM*, 2007.
- [22] IEEE Std. 519-1992, IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems.



Bhim Singh

He was born in Rahamapur (UP), India, in 1956. He received his B.E (Electrical) degree from the University of Roorkee, Roorkee, India, in 1977, and his M.Tech. and Ph.D. degrees from the Indian Institute of Technology (IIT) Delhi, New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a Lecturer, and in 1988 became a Reader. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, as an Assistant Professor. He became an Associate Professor in 1994 and Full Professor in 1997. His areas of interest include power electronics, electrical machines and drives, active filters, FACTS, HVDC, and power quality. Dr. Singh is a Fellow of the Indian National Academy of Engineering (INAE), the Institution of Engineers (India) (IE(I)), and the Institution of Electronics and Telecommunication Engineers (IETE), a Life Member of the Indian Society for Technical Education (ISTE), the System Society of India (SSI), and the National Institution of Quality and Reliability (NIQR), and a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).

**R. Saha**

He received his Bachelor of Electrical Engineering (B.E.E.) and Master of Electrical Engineering (M.E.E.) degrees from Jadavpur University, Kolkata, India, in 1980 and 1982, respectively and his Ph.D. from the Indian Institute of Technology (IIT) Delhi, New Delhi, India, in 2007. He worked as a Software Engineer in the R&D wing of the MMC Digital System Division, India, from 1982 to 1983. He joined Central Electricity Authority (CEA), Govt. of India, in Nov'83 through Central Power Engineering Service (Group-A). He has been associated with the Planning of National Transmission Grid in India and related System Studies for Integrated Grid Operation & Control and Management. His field of interest includes Power Electronics and FACTS technology. He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).